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MS-7B24

mATX
Ver: 1.020

PC MATE BAZOOKA

Coffeelake Platform

CPU: Coffeelake S

PCH H370B360

SPI ROM: 128MB

Memory: DDR4* 4(Dual Channel)

Power Solution

CPU: RI3607

VCCSA: RI8125E

VCCIO: SY8288

DDR: RI8125E

PCH: RI8125E

ACPE MPS

Onboard Chip

LAN RIL8111H

Dual Codec: ALC887

SIO: NCIG797/6795D

Type C: ASM1543

USB3 Redrive: NB7VPQ702X1

GPIO: NCI5605* 2

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

M2 Slot (Socket 1) * 1

LED

EZ Debug LED

Audio Line LED

BOT LED

Rear I/O Connectors

PS2

USB2.0x2

USB3.1 Gen1x2

RJ45+ USB3.1 (Type C+ A)

Audio Jack 3Port

HDMI+ (DVI/DVI+VGA)

Internal Connectors

Dual SATA * 1

SINGLE SATA * 4

FUSE30 Header* 1

FUSE20 Header* 2

Front Audio Header* 1

Front Panel Header* 2

SPI Header* 1

TPM Header* 1

CPU Fan * 1

System Fan * 2

Internal Pin Header

JRGB1

JSPI1

JIBT1

JBAT1

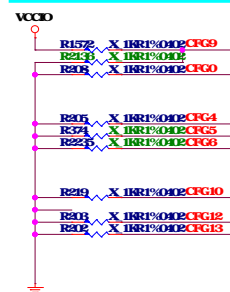
JCI1

JTPM1

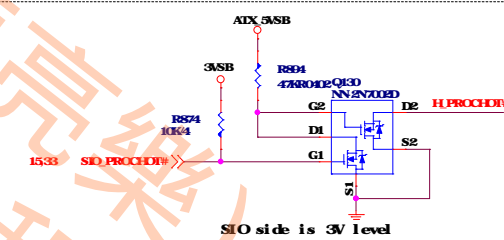
JCOM1

JLPT1

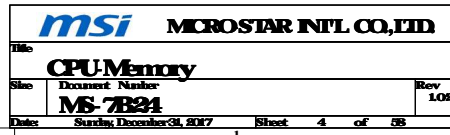
msi MICROSTAR INT'L CO., LTD.	
Title Cover Sheet	
Doc No	Doc No
MS-7B24	
Date	Rev
Sunday, December 31, 2017	1.020
Sheet 1 of 58	

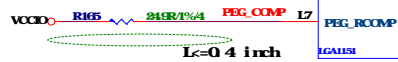
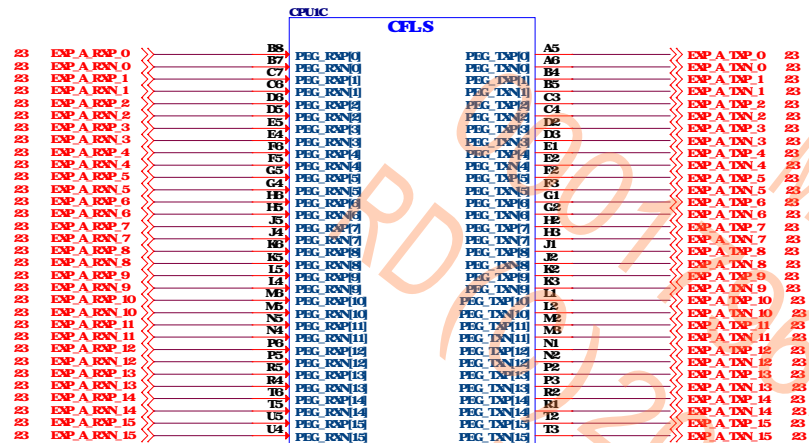


ZIF-SOCKET1151-HF
N12 151A030 F02

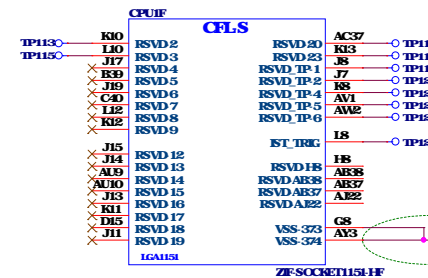


OCG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	FCU R/L Lock
1			RSND
2	NORM	REVERSE	REG. LANE, REVERSE/L
3			RSND
4	DISABLE	ENABLE	SLP
5	DISABLE	ENABLE	PRCLOCK[0]
6	DISABLE	ENABLE	PRCLOCK[1]
7	RESET#	HC (S. REQ)	REG. DEFERR. TRAINING
8			RSND
9	PRESENT#	NO PRESENT#	SMD PRESENT#
10			RSND
11			RSND
12			RSND
13			RSND
14			RSND
15			RSND
16			RSND
17			RSND
18			RSND
19			RSND





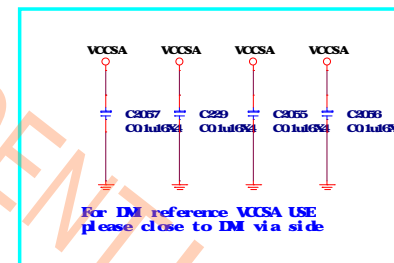
IGA1151
ZF-SOCKET1151-HF
N12 151A080F02



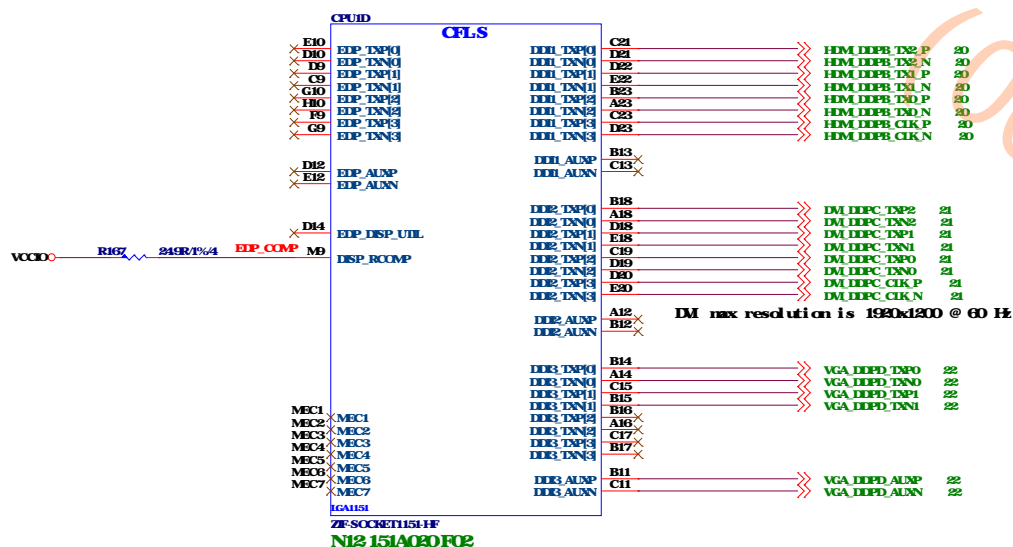
N12 151A080F02

2017/7/12

GS and AX3 can connect directly by Q18 1.0

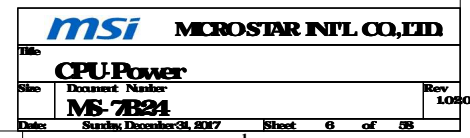
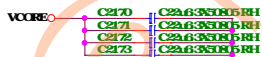


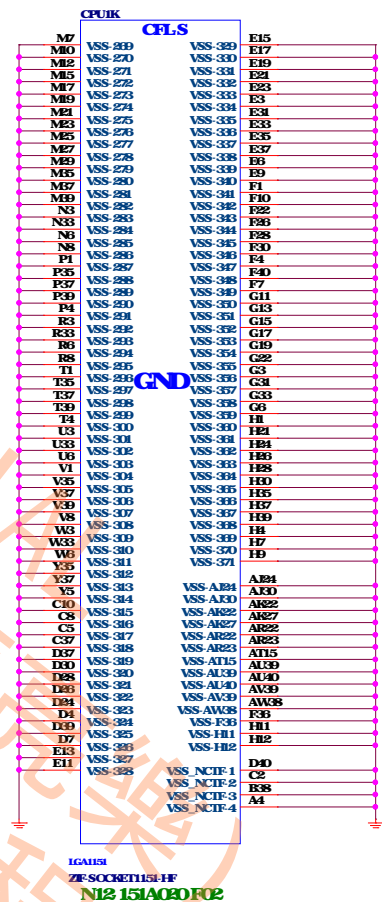
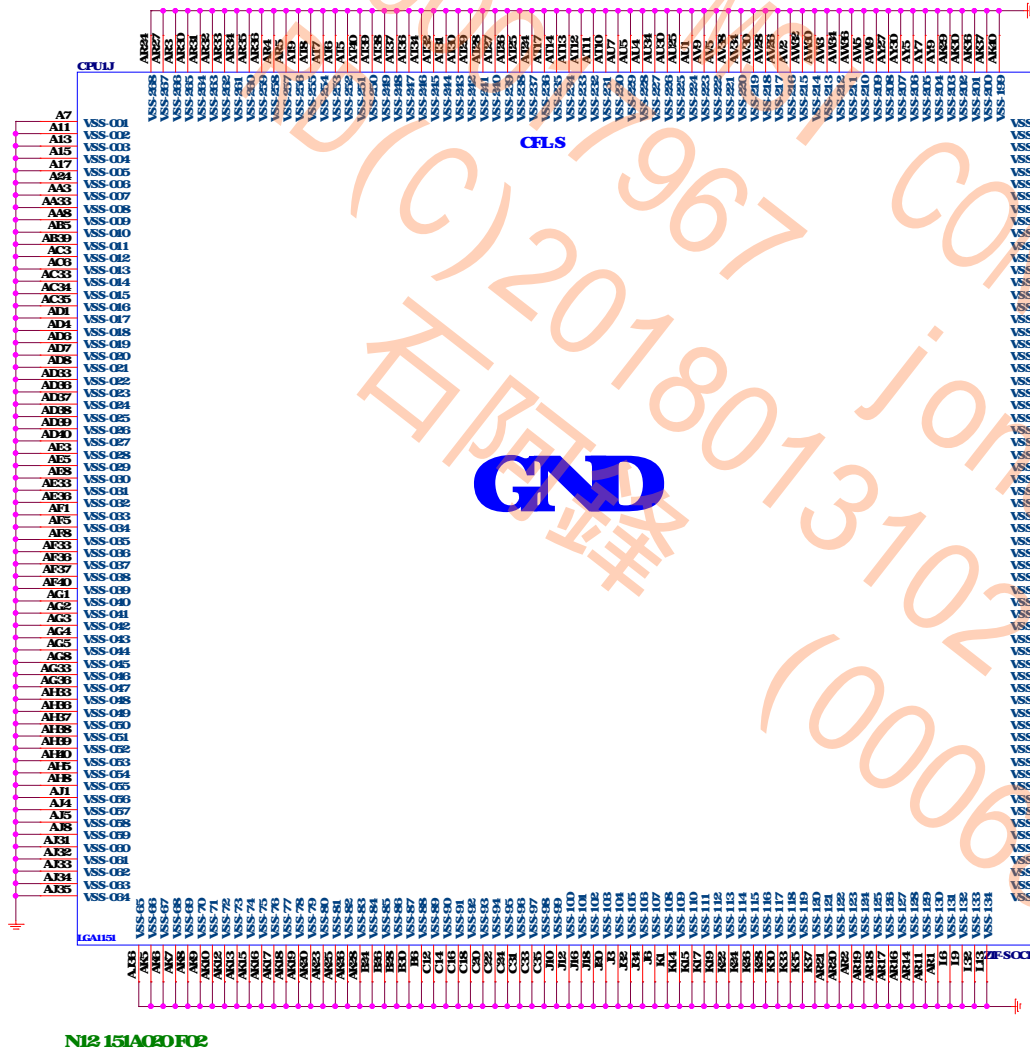
2017013 Review ADD



MEC1
MEC2
MEC3
MEC4
MEC5
MEC6
MEC7

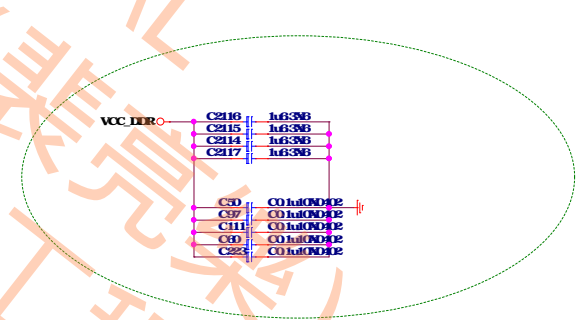
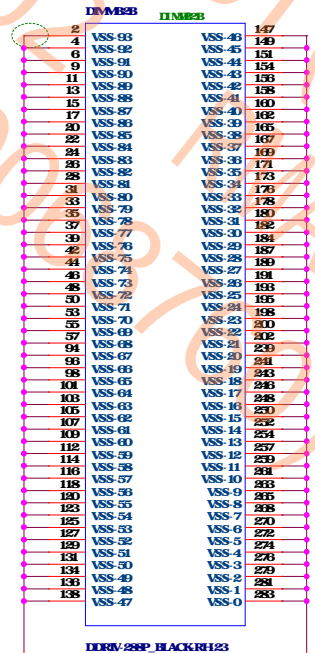
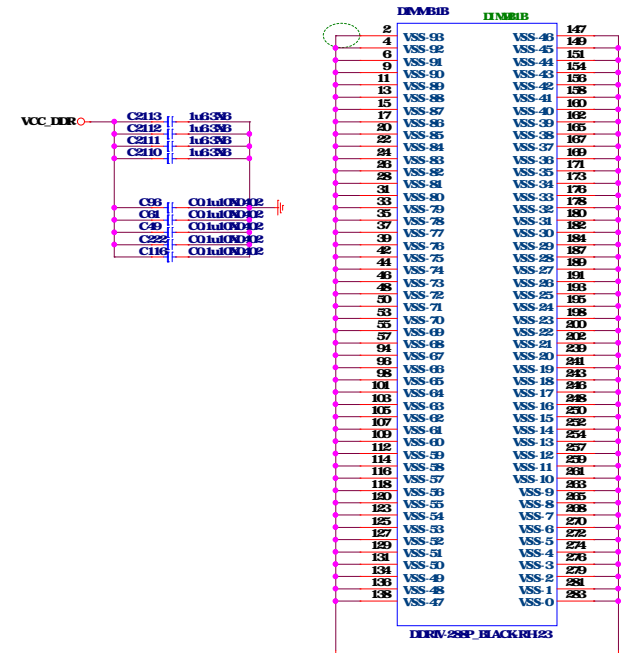
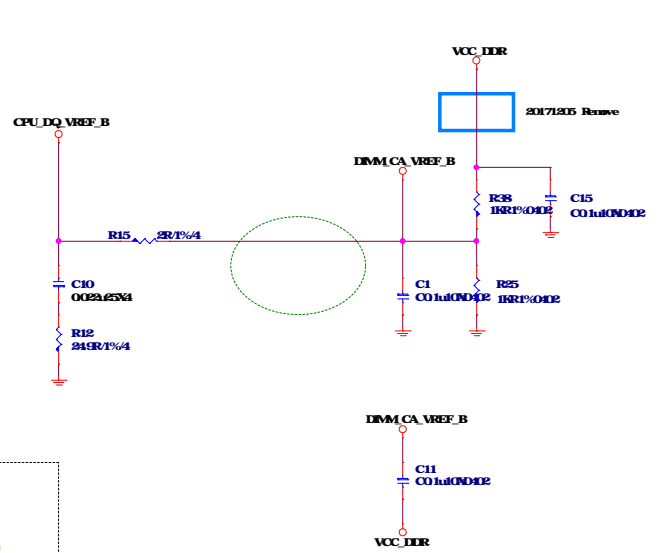
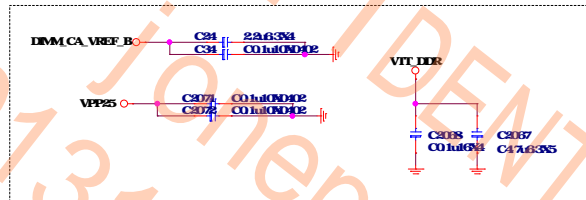
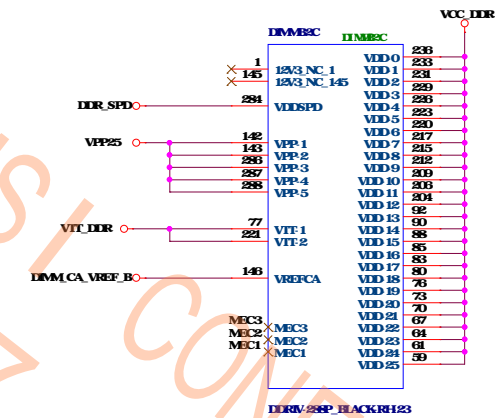
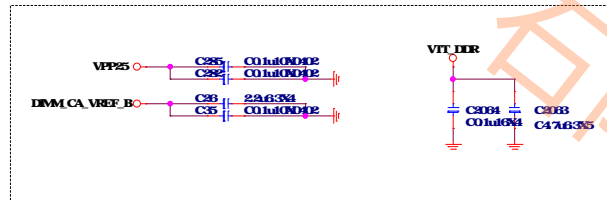
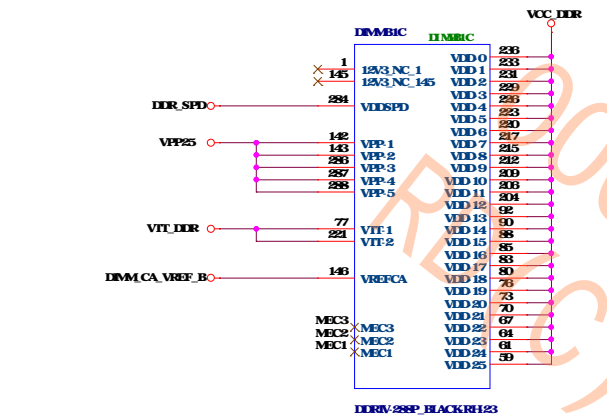
IGA1151
ZF-SOCKET1151-HF
N12 151A080F02





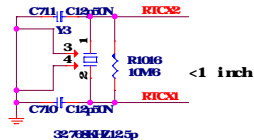




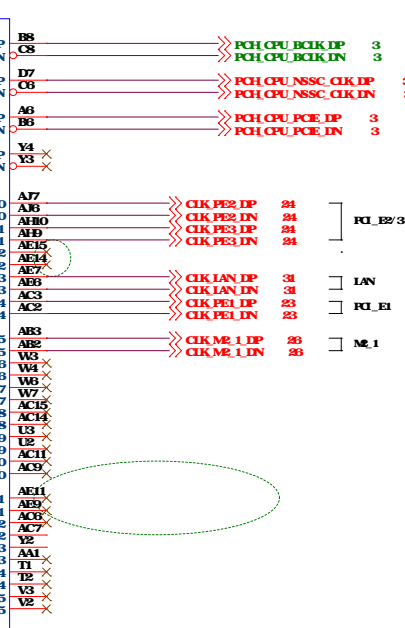
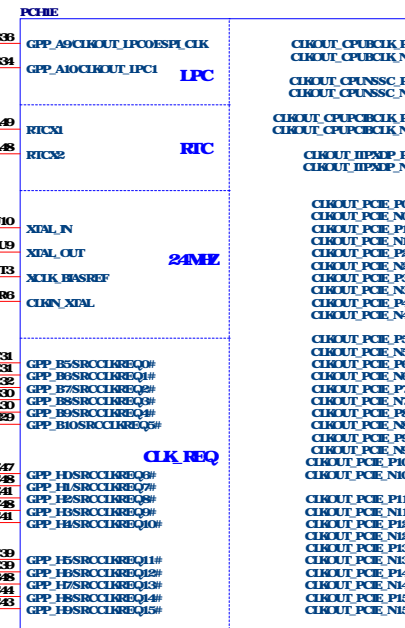
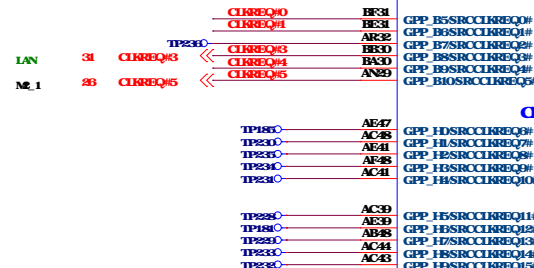
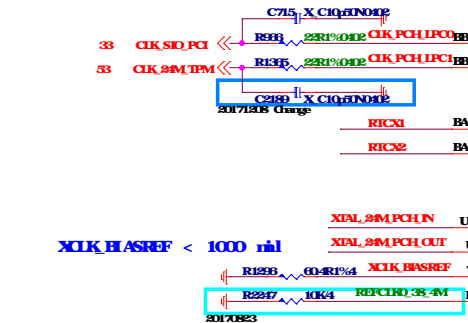
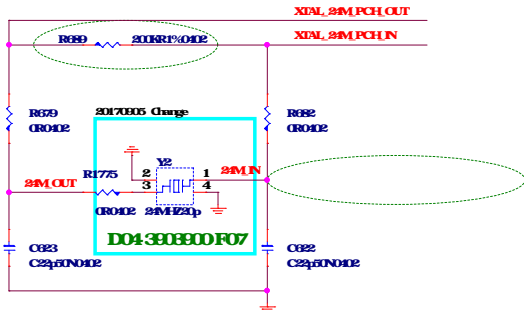


PCH_CLK

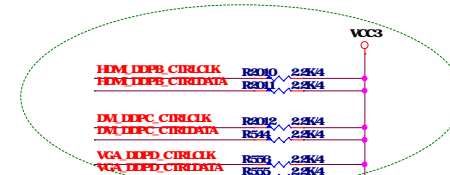
Close to PCH



2017/7/11
The value of R689 is the same as FIG r09 by Intel's feedback



PCHH
0B1-7B53002106



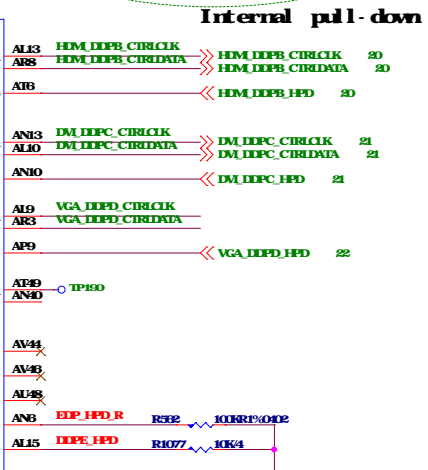
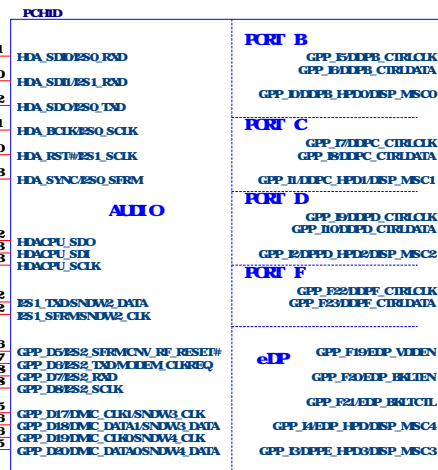
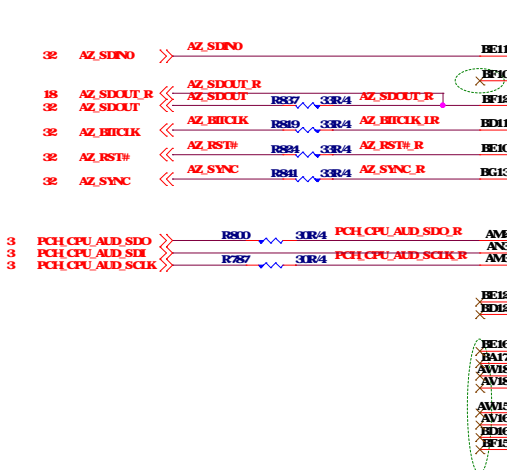
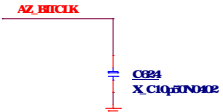
Internal pull-down is disabled after PCHPWCK is high

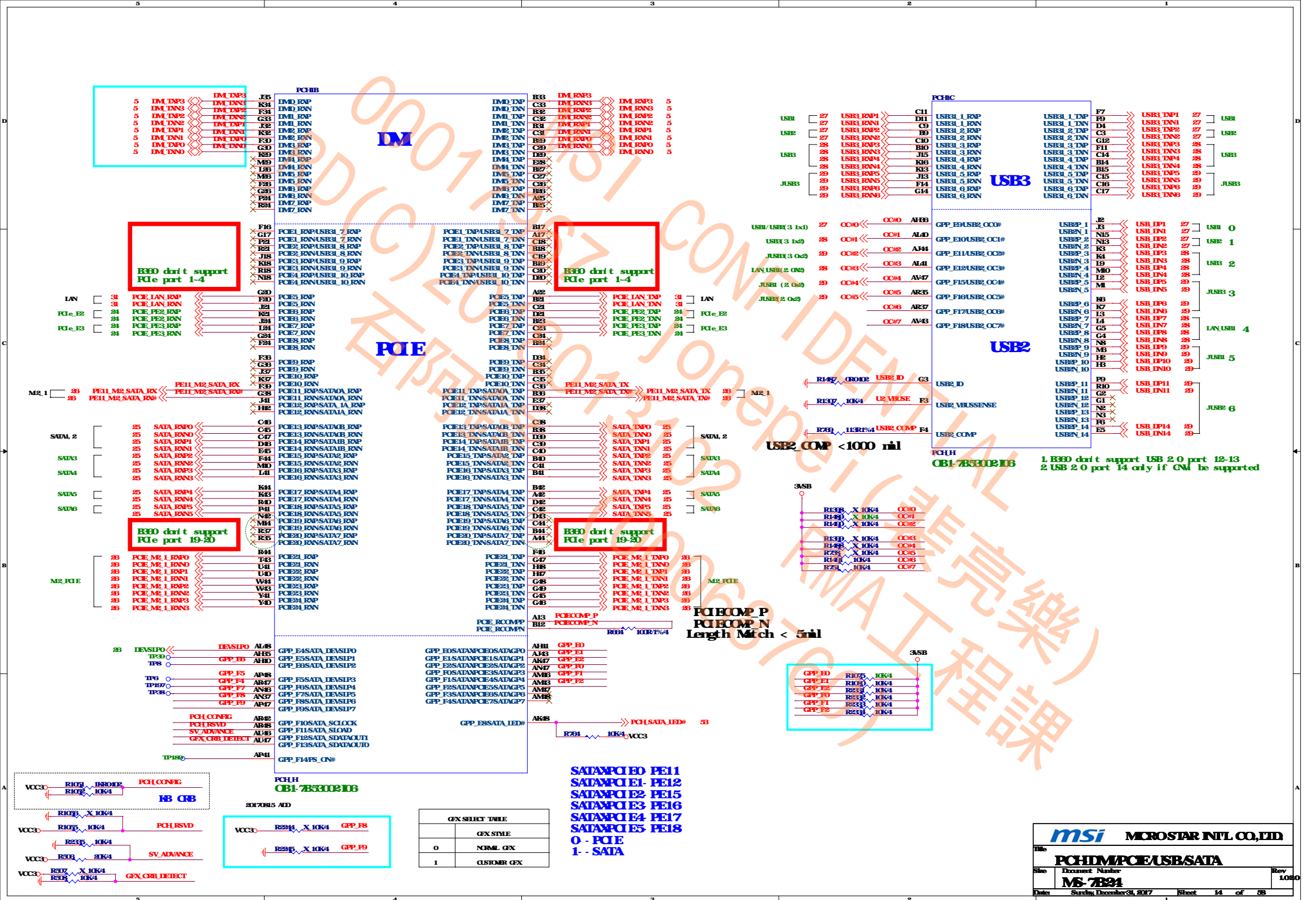
0 : Port B is not detected (Default)
1 : Port B is detected

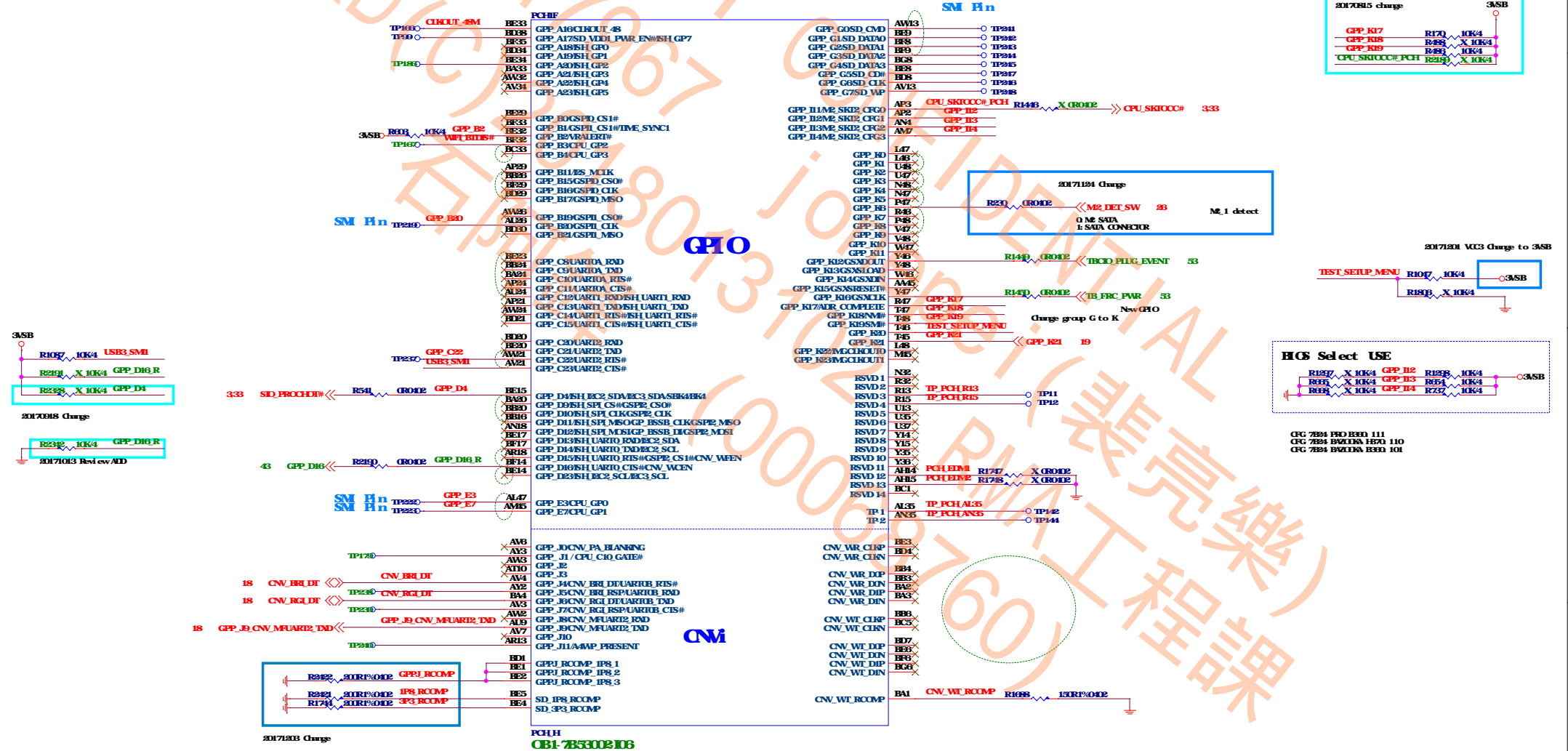
0 : Port C is not detected (Default)
1 : Port C is detected

0 : Port D is not detected (Default)
1 : Port D is detected

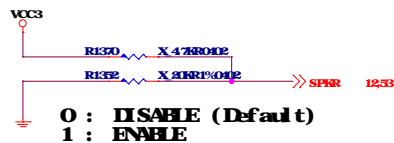
PCH_AUDIO





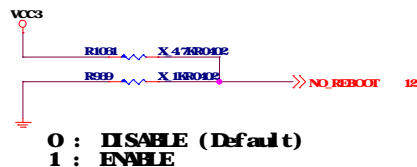


TOP Swap



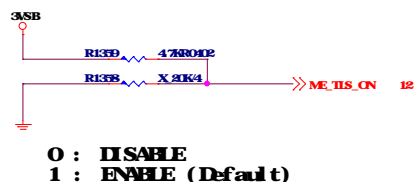
Internal pull-down is disabled after PCH_PWCK is high

No Reboot



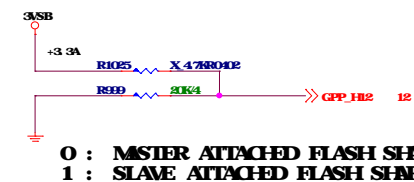
Internal pull-down is disabled after PCH_PWCK is high

TLS confidentiality



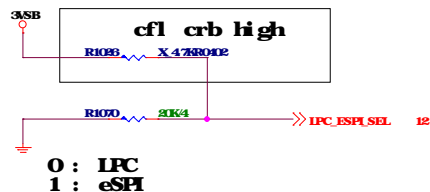
Internal pull-down is disabled after RSMST# de-assert.

ESPI FLASH SHARING MODE



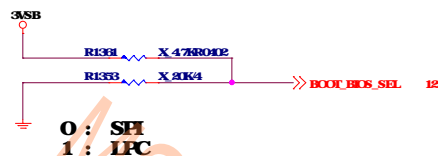
Internal pull-down is disabled after RSMST# de-assert.

LPC eSPI Mode



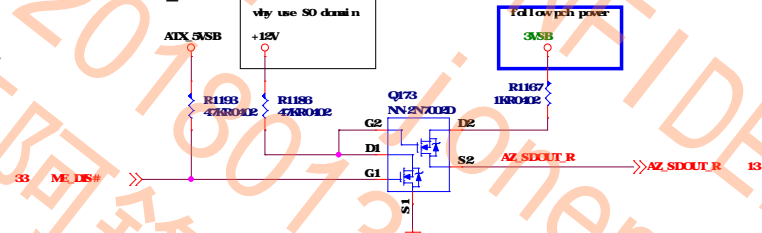
Internal pull-down is disabled after RSMST# de-assert.

Boot HCS



Internal pull-down is disabled after PCH_PWCK is high

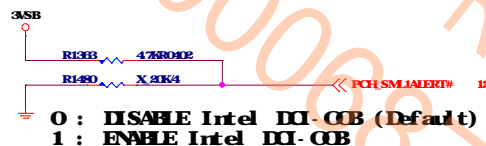
HDA_SDO



0 : Enable security measures defined in the Flash Descriptor.
(Default)
1 : DISABLE Flash Descriptor Security(Override).

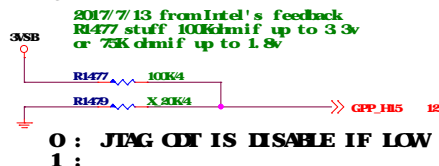
Internal pull-down is disabled after PCH_PWCK is high

DI ENABLE

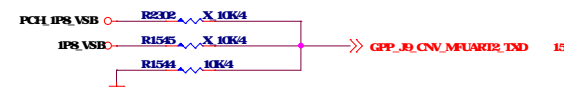


Internal pull-down is disabled after RSMST# de-assert.

ODT DISABLE



SELECT THE SPI HCS FLASH INTERFACE OPERATING VOLTAGE



0 = VCCSPI IS CONNECTED TO 3.3V RAIL (DEFAULT)
1 = VCCSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD

201704 CHINE

XIAL FREQUENCY SELECTION

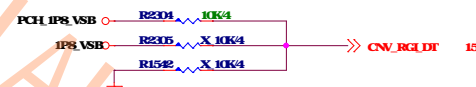


1 = 24MHZ (25MHZ WHEN XIAL_FREQ_DIVIDER NON ZERO)
0 = 38.4/19.2MHZ

XIAL_SEL1 : Internal Pull down

MODEM AND NFC REFERENCE CLOCK SOURCE SELECT

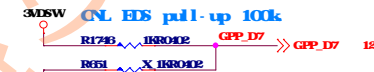
2017/7/12 from Intel's feedback
FU if the integrated CNM is enabled
PD if the integrated CNM is disabled



CNM_BS
0 = Integrated CNM enable
1 = Integrated CNM disable

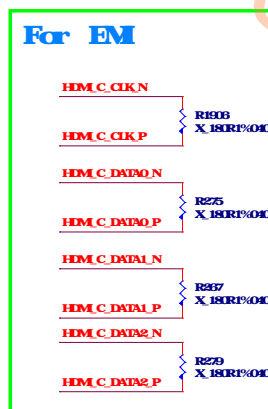
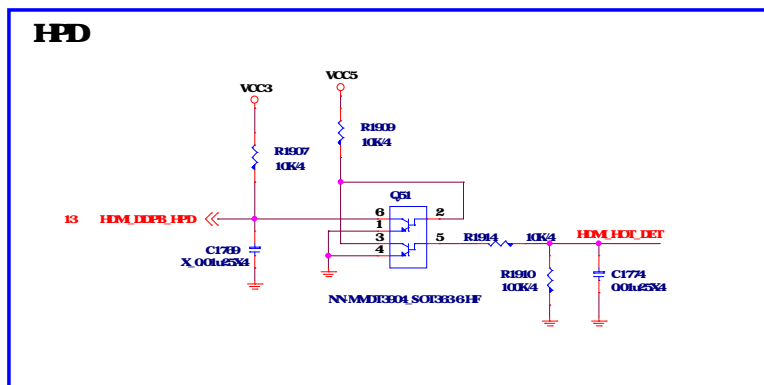
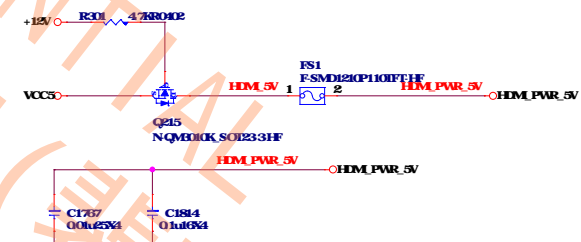
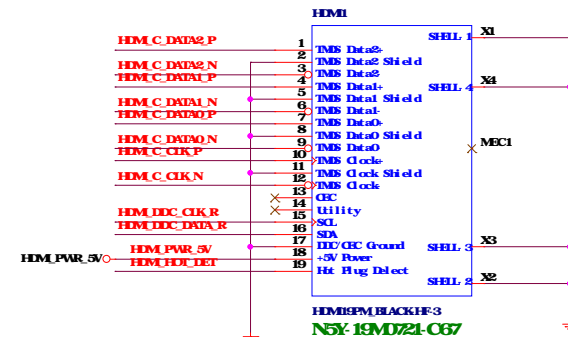
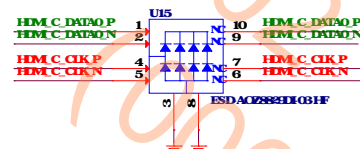
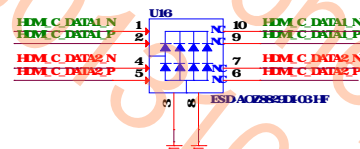
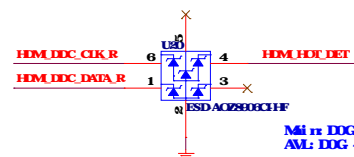
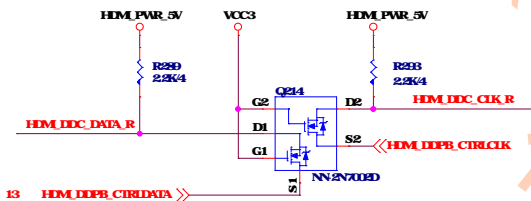
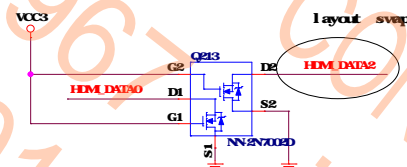
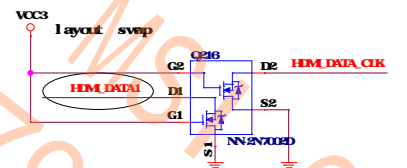
20170816 change

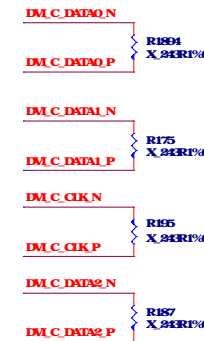
XIAL INPUT MODE



1 = XIAL INPUT IS DIFFERENTIAL
0 = XIAL INPUT IS SINGLE ENDED
PCH HAS INTERNAL 20K PD

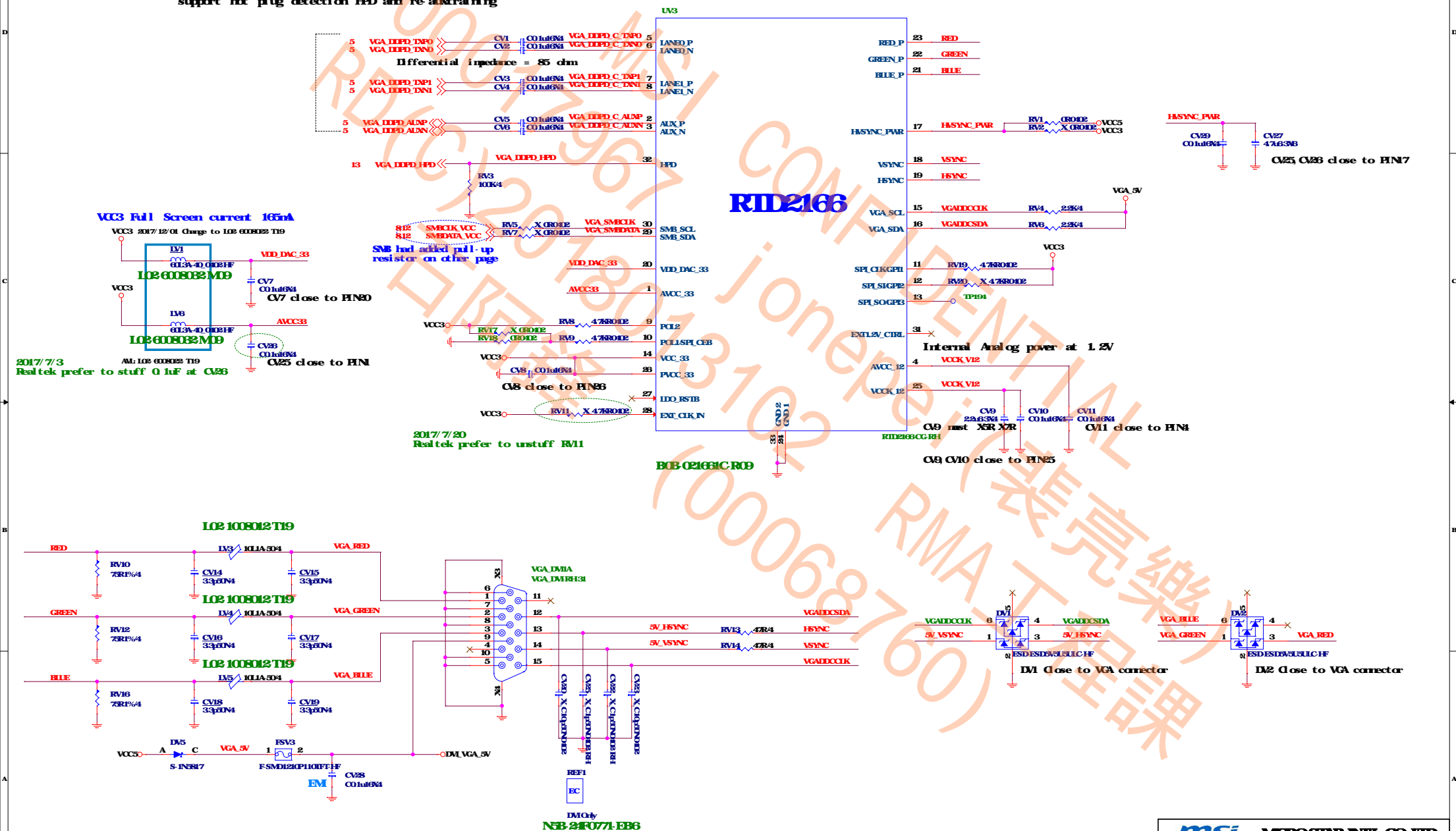
HMI, DM : 1920x1200 at 60 Hz (16 10 W/VA)

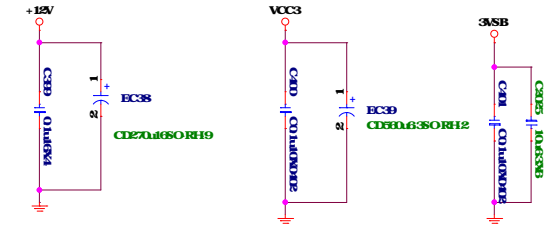
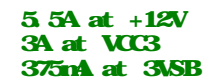




Note:

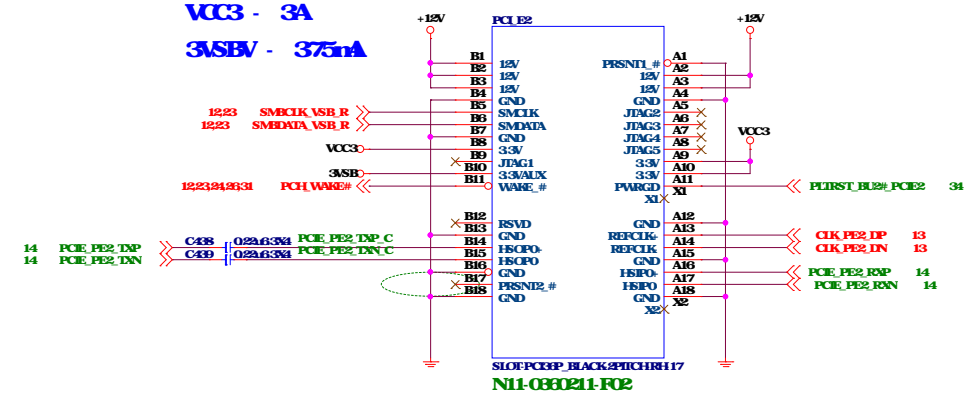
If connect to eDP port, must confirm whether it support hot plug detection HPD and re-audstraining



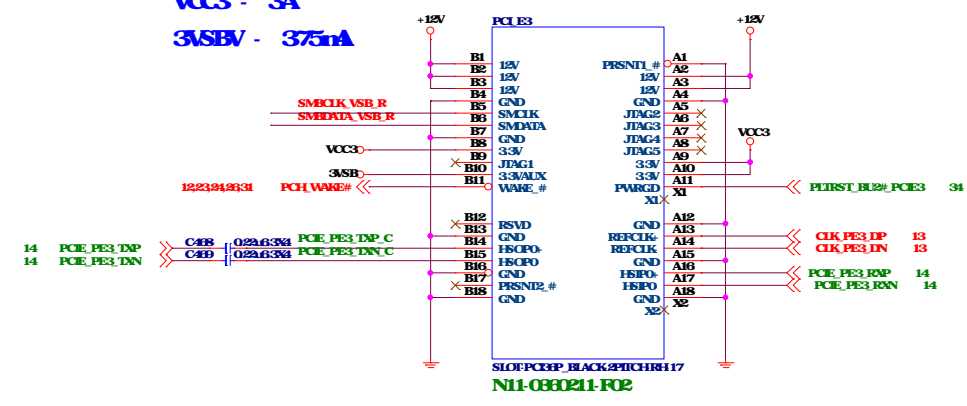


PCH PCIe X1 Slot

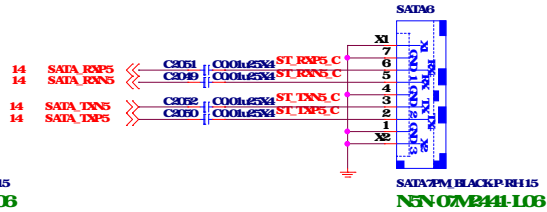
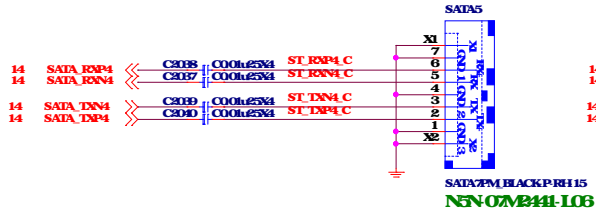
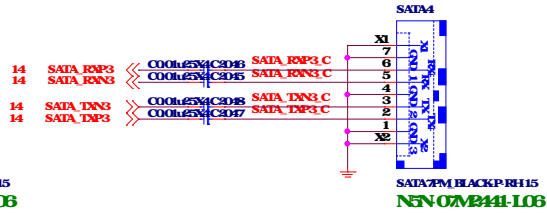
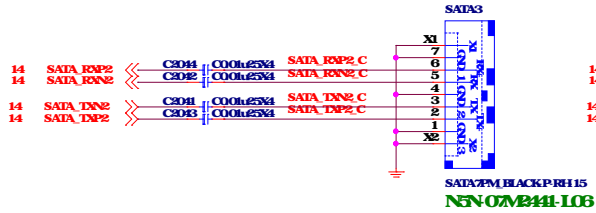
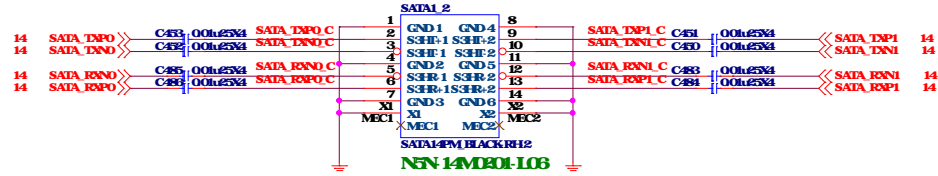
12V - 0.5A
VCC3 - 3A
3.3SBV - 375mA

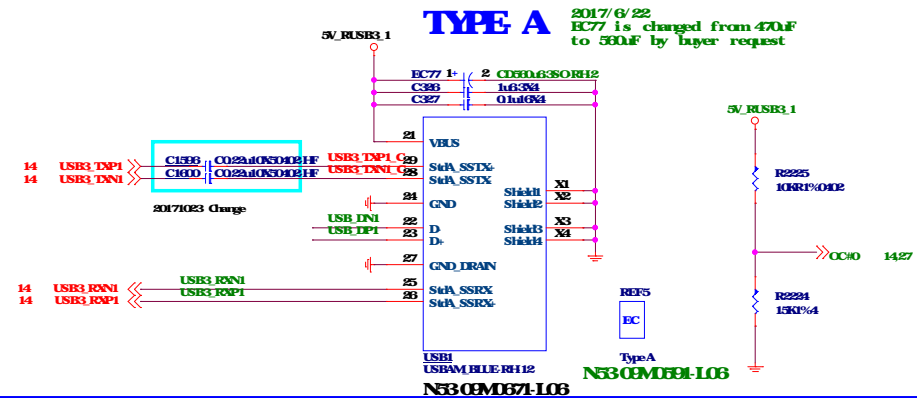


12V - 0.5A
VCC3 - 3A
3.3SBV - 375mA

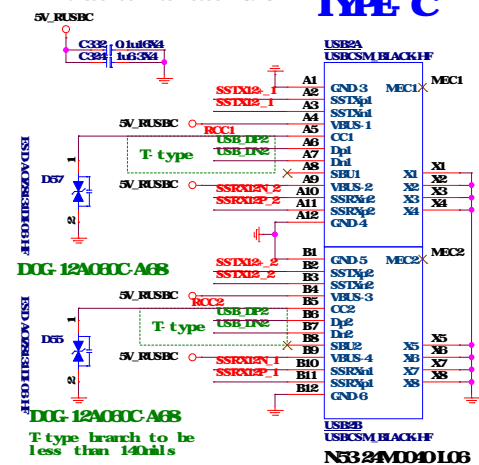
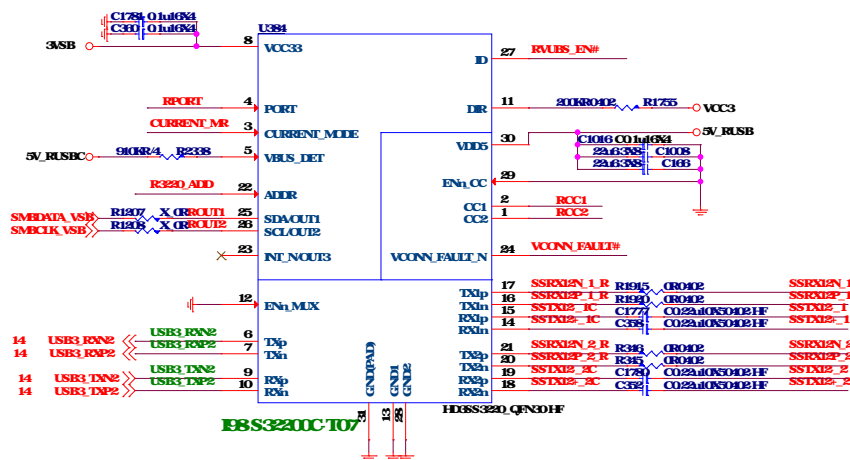


SATA6G PORT01

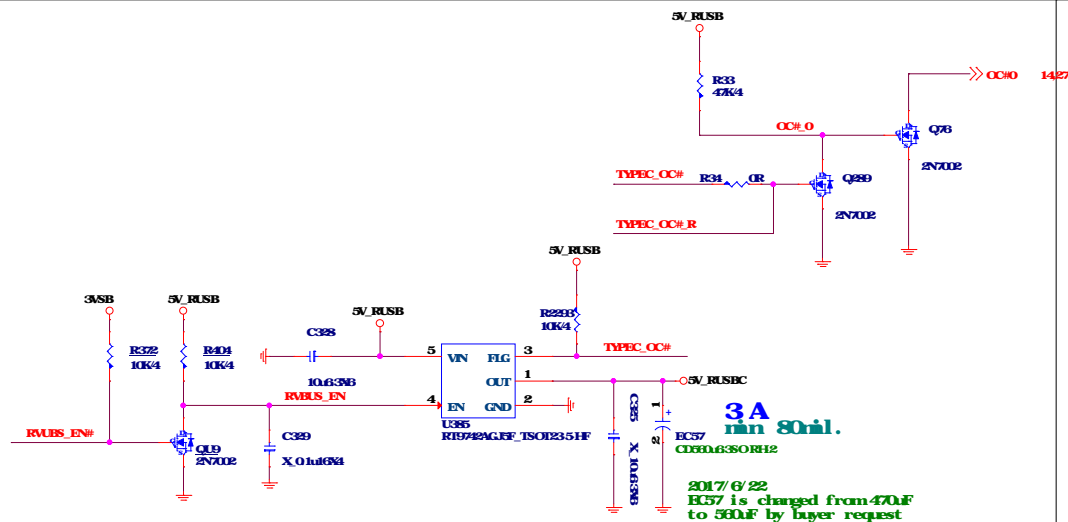


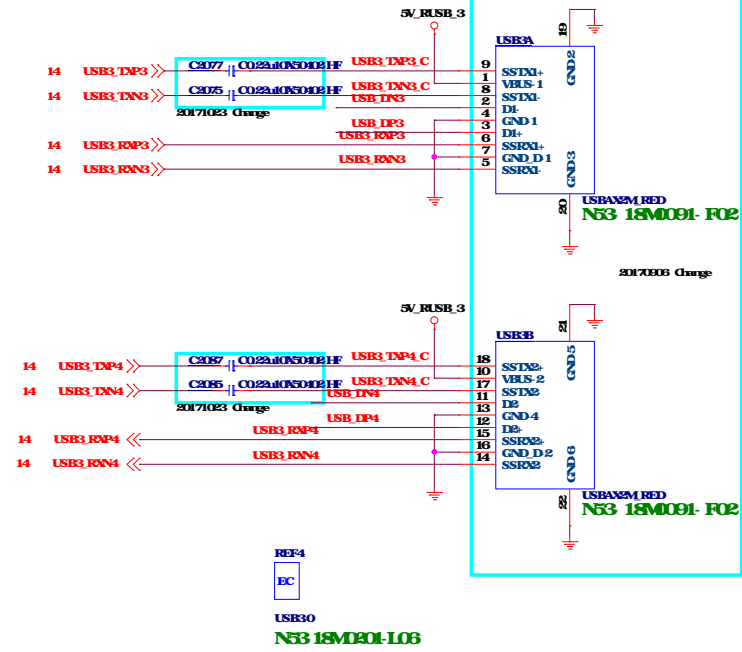
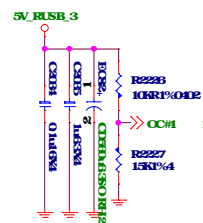
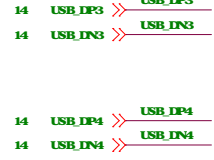
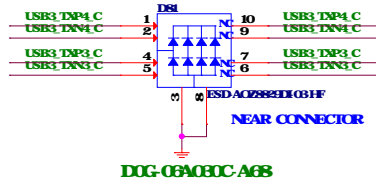
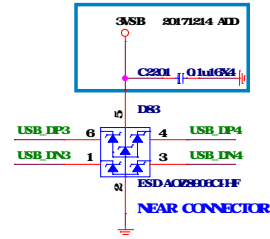
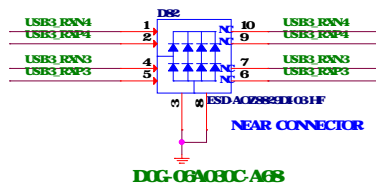


close to Connector USB5 **TYPE C**

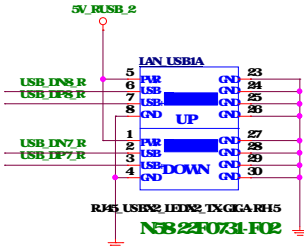
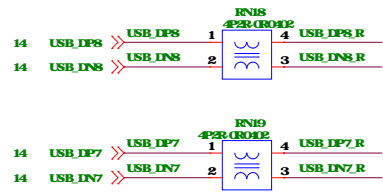


L - Default for 900mA
M- Mid (500K) for 1.5A
H- High (10K) for 3A

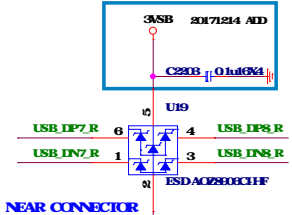
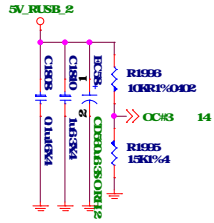


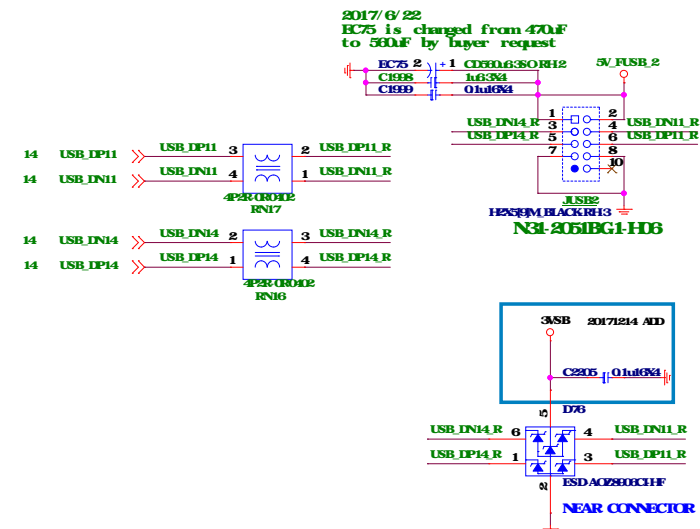
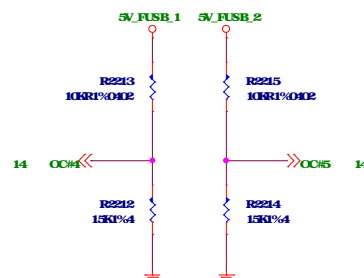
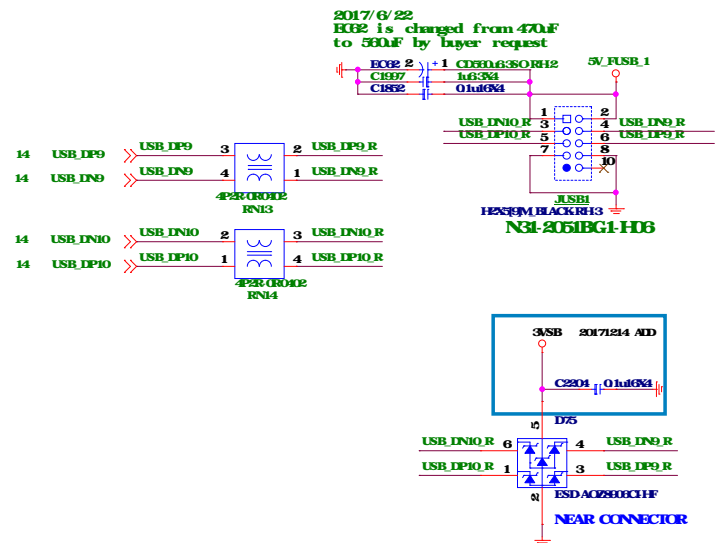


LAN_USB1

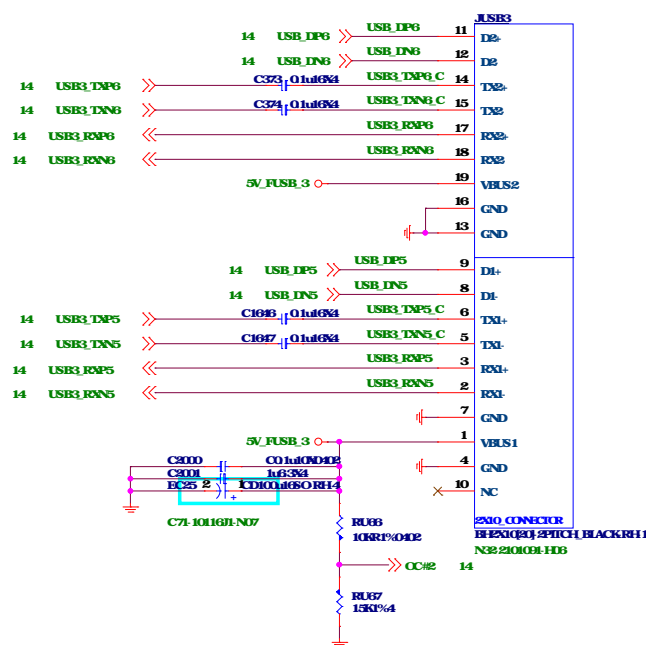
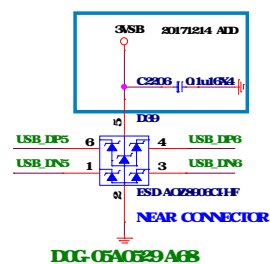
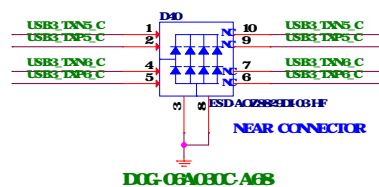
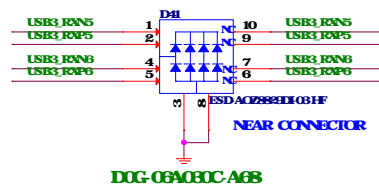


2017/6/22
EC58 is changed from 470uF
to 560uF by buyer request

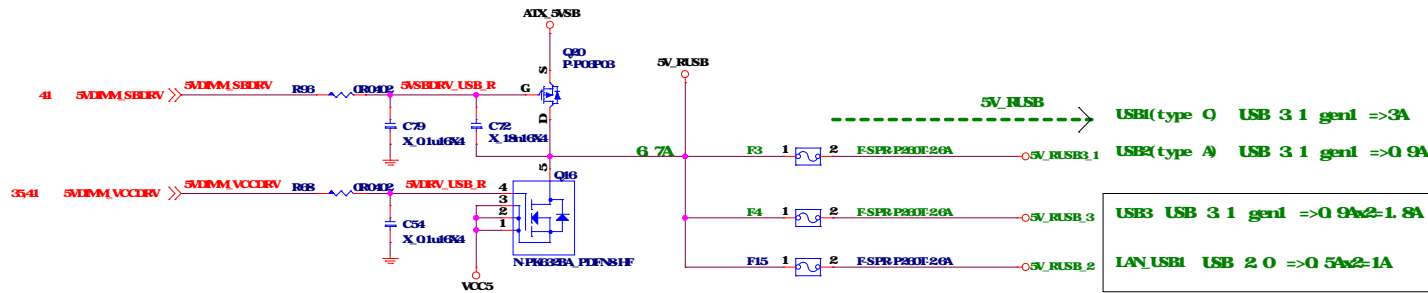


FRONT USB20

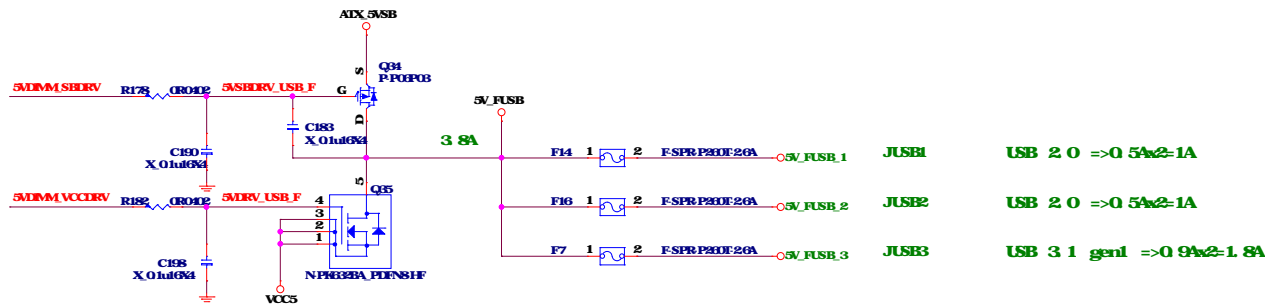
FRONT USB30

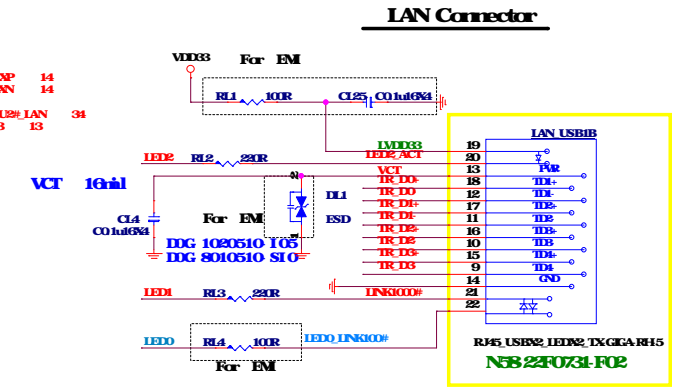


REAR USB PORT POWER



FRONT USB PORT POWER



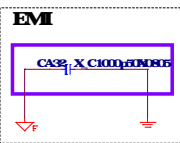
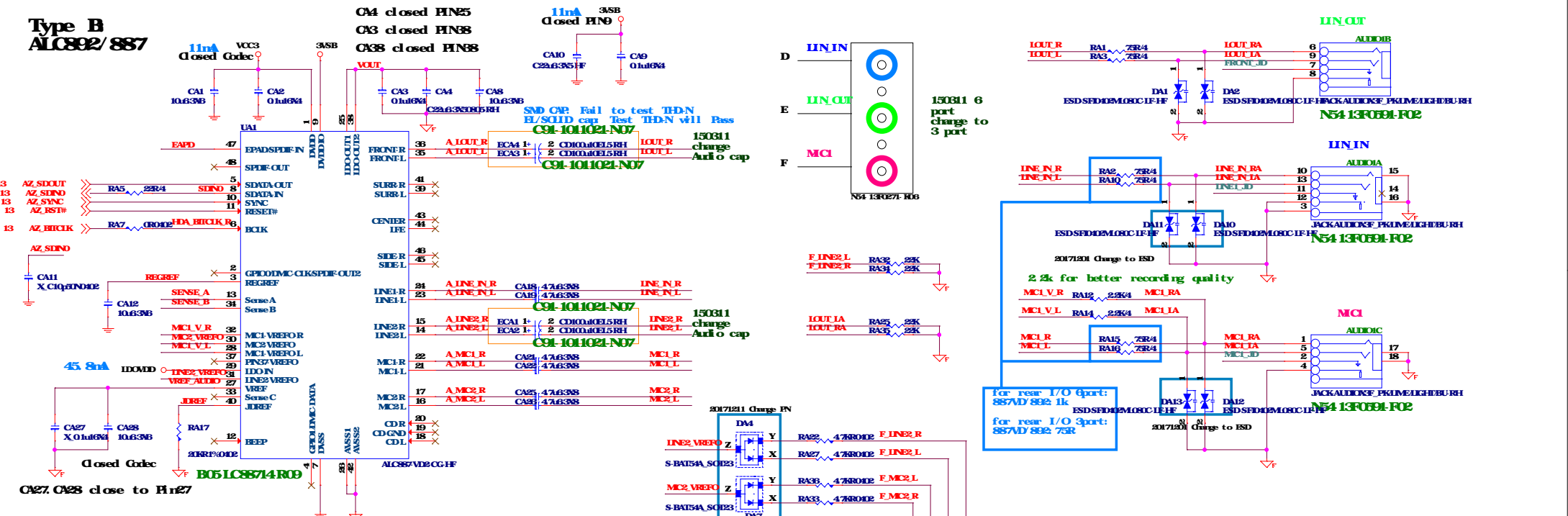
8111H B06 08111CC R09
8111G B06 081116C R09

The diagram shows a common anode LED configuration. Three LEDs are connected to a common anode (5V). The cathodes are connected to pins C12, C13, and C15, which are also labeled C10Q2ANODE. The LEDs are labeled LED1, ACT, LED2, and UNK100#.

	3.3V @ nA	nW
10 MIdle/E&k	17.15/116.7	56.6/385.1
100 MIdle/E&k	71.45/129.5	235.8/427.4
Gga Idle/E&k	179.1/243.9	591/804.9
ALPS	6.41	21.15

	3 V @ nA	nW
10 MId e/Tb&	9 9/84 69	32 67/279 48
100 MId e/Tb&	48 11/92 44	158 76/305 0
Gga Id e/Tb&	124 5/177 57	410 85/585 9
ADDS	5 50	18 15

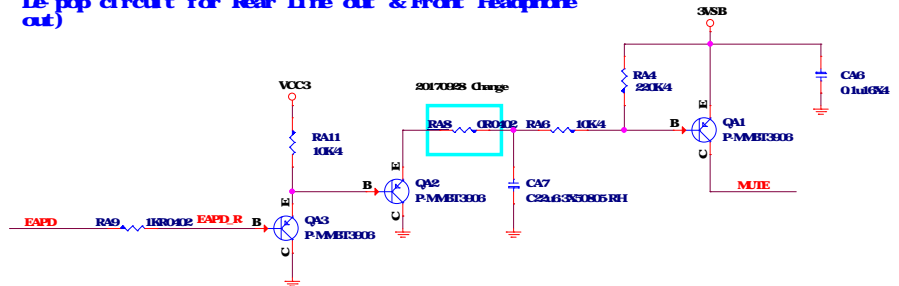
Type B ALC887 / 887



package 0 5

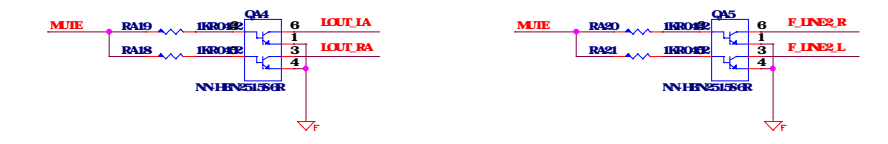
Rear Line OUT De POP circuit

De pop circuit for Rear Line out & Front Headphone out)

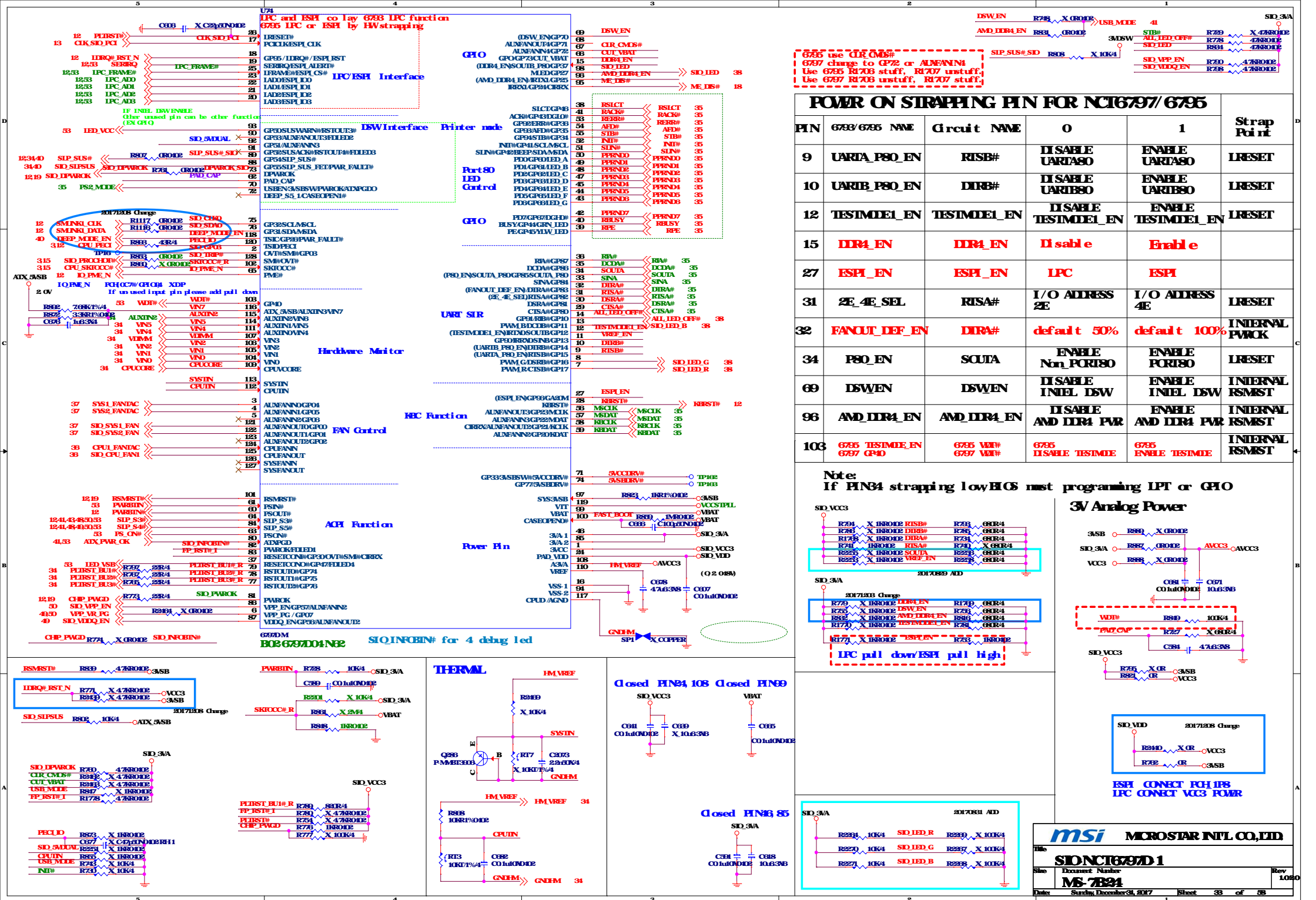


Digital

Anal og

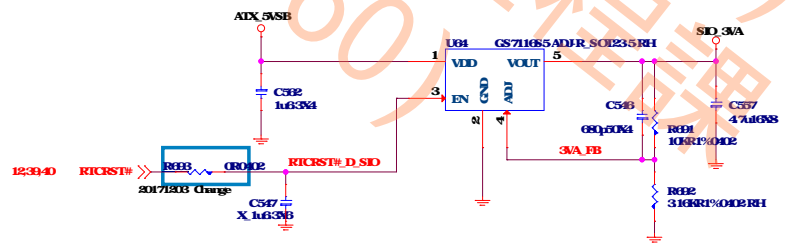
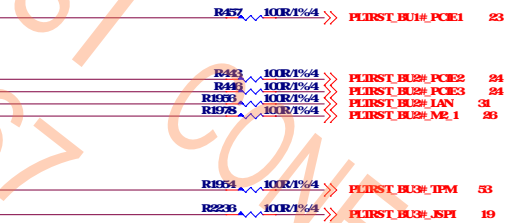
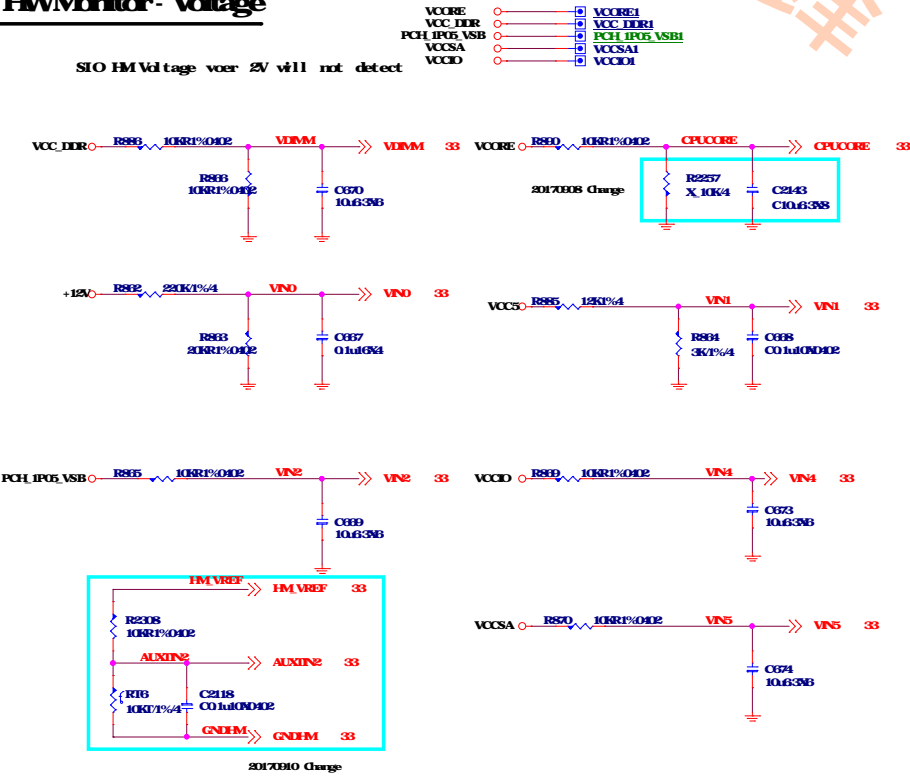


Varistor --- cap for cost down
DGG 2960600 S10
DGG 3010610 105
Close to Jack



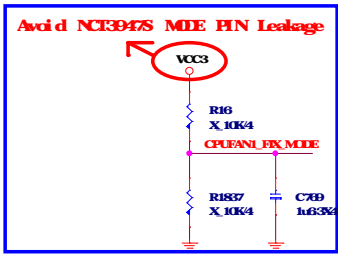
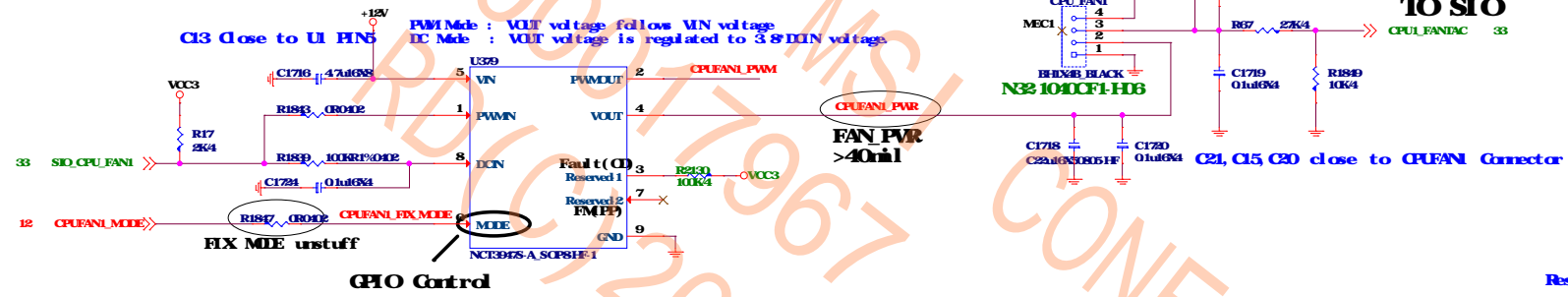
00017967 MSI
RD(C) 2018013102 jonepei (裴亮樂)
石阿鋒 RMA 工程師 (00068760)

HWMonitor- Voltage



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MDE

- 1. PWM/DC/OPP LED RC/B3 L B
- 2. GPIO HS PW MDC MODE
- 3. OCP GPD BDS
- 4. PWM OR DC FAN GPD BDS
- 5. FAN S SOFTWARE GPIO



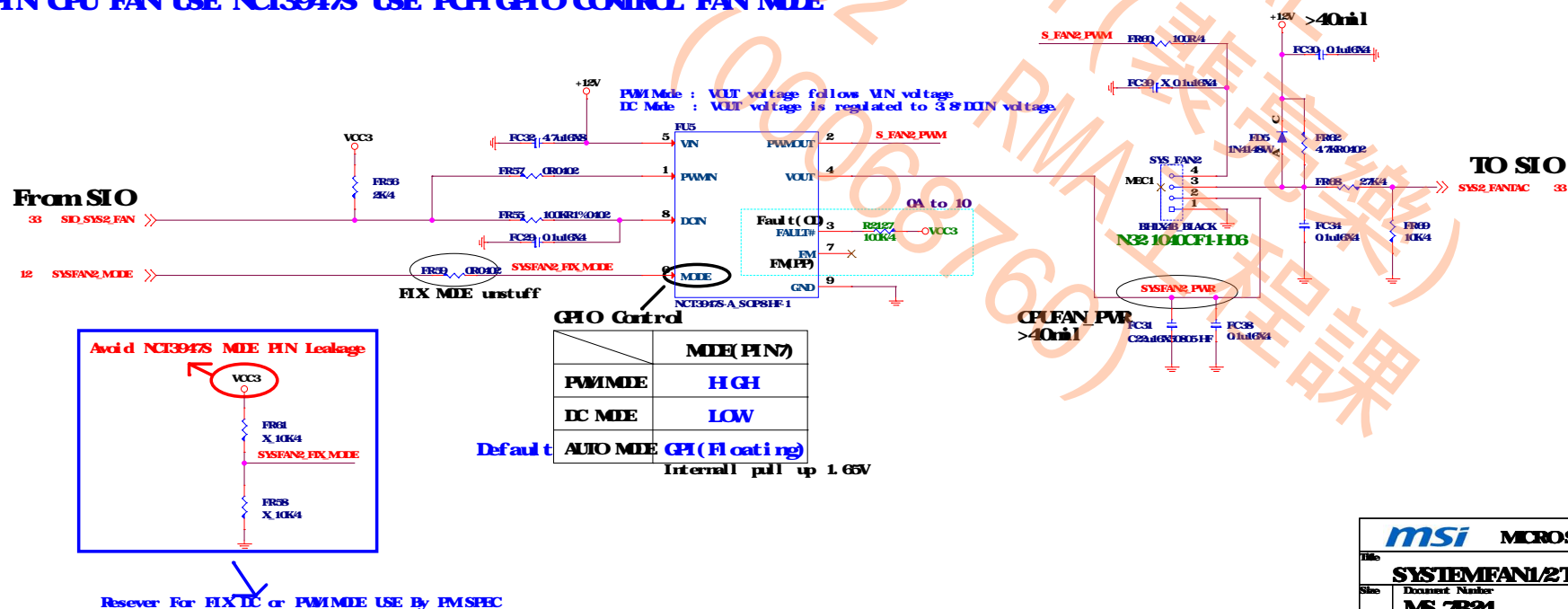
Reverse For FIX DC or PWM MDE USE By PMSPEC

GPIO Control

	MDE (PIN7)
PWM MDE	HIGH
DC MDE	LOW
Default AUTO MDE	GPIO (Floating)

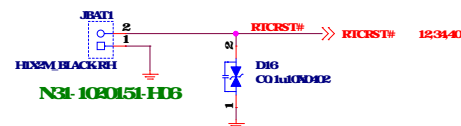
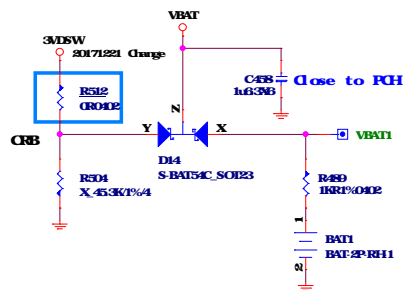
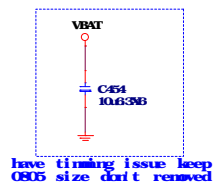
Internal pull up 1.65V

TYPE K: 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

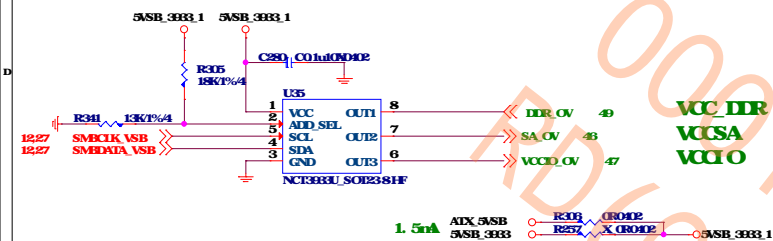


MSI CONFIDENTIAL
RD(C)2018013102
石阿鋒 jonepei (裴亮樂)
RMA工程課 (00068760)

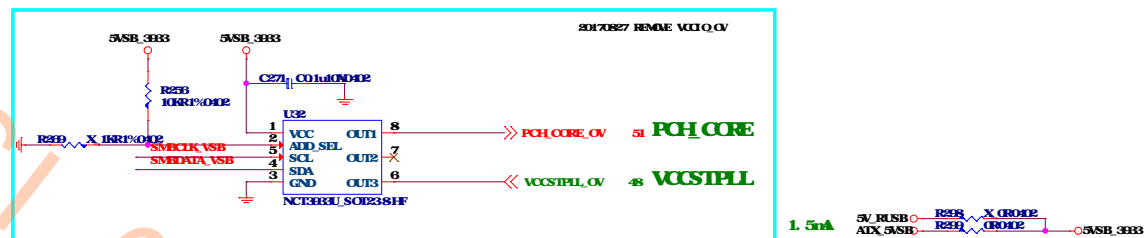
VBAT



Q26 RH=18K RL=13K



0x20 RH=10K RL=OPEN



The schematic diagram illustrates the internal circuitry of the OT7-B1703-SF9 power management IC. The IC is shown in a package with pins 1 through 14. The diagram includes various control pins, power pins, and signal pins. Key components include resistors (R1-R10), capacitors (C1-C4), and transistors (Q1, Q4). The diagram is labeled with 'OT7-B1703-SF9' at the bottom.

Pin 1: 3VSW, VDD

Pin 2: 3VSW_PARGD, 3VSW_DET

Pin 3: DEEP_MODE_EN

Pin 4: AIX_5VSB, AIX_5VSB_DET

Pin 5: SLP_SUS#, SLP_SUS#

Pin 6: VRM_VRDY, VRM_PGD

Pin 7: VRM_LEN, VRM_LEN

Pin 8: LO5VSB, VSB_DET

Pin 9: GND

Pin 10: RICRST_DET, RICRST

Pin 11: VSB_EN#, VSB_ENABLE#

Pin 12: DPWRCK_SLG, DPWRCK_SLG

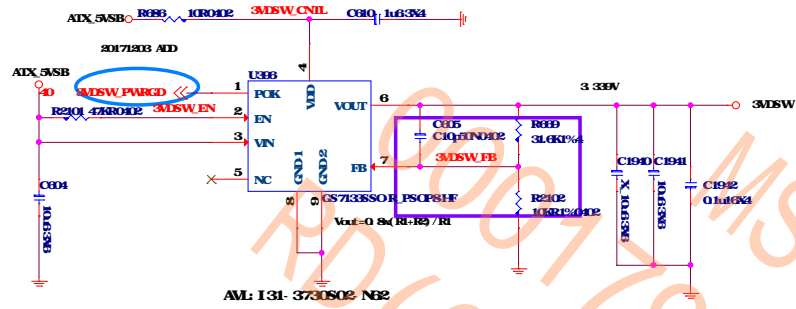
Pin 13: RSMRST_SLG, RSMRST_SLG

Pin 14: PWRRCK_SLG

Internal Components:

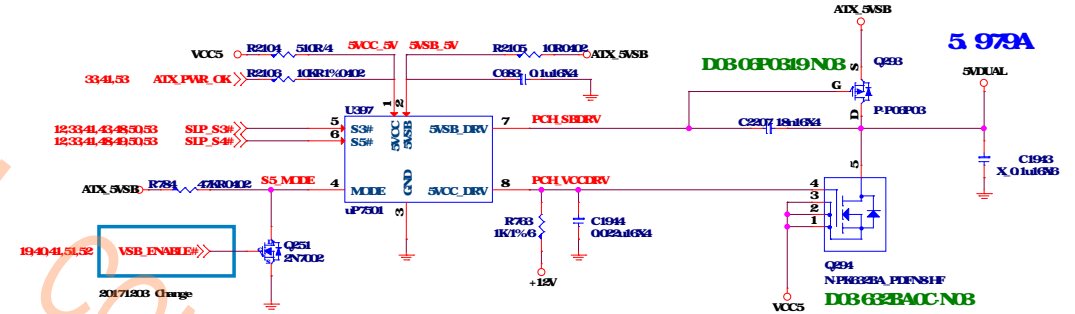
- Resistors: R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100.
- Capacitors: C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100.
- Transistors: Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24, Q25, Q26, Q27, Q28, Q29, Q30, Q31, Q32, Q33, Q34, Q35, Q36, Q37, Q38, Q39, Q40, Q41, Q42, Q43, Q44, Q45, Q46, Q47, Q48, Q49, Q50, Q51, Q52, Q53, Q54, Q55, Q56, Q57, Q58, Q59, Q60, Q61, Q62, Q63, Q64, Q65, Q66, Q67, Q68, Q69, Q70, Q71, Q72, Q73, Q74, Q75, Q76, Q77, Q78, Q79, Q80, Q81, Q82, Q83, Q84, Q85, Q86, Q87, Q88, Q89, Q90, Q91, Q92, Q93, Q94, Q95, Q96, Q97, Q98, Q99, Q100.

3MDSW

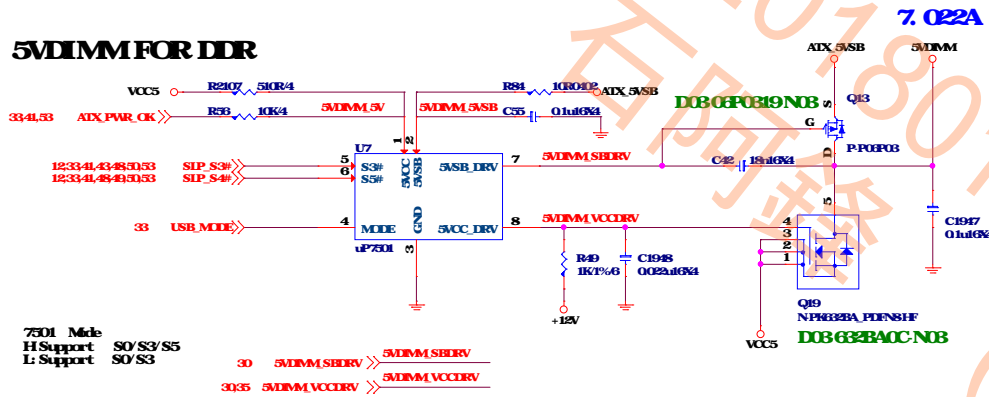


5VDUAL

5VDUAL is power source of 1F0SB



5VDIMM FOR DDR



$$FB-VIN [R2447 / (R2447 + R2446)] = 5V [3.3K / 5.5K] = 3V$$

19-01-01-01-01

USB_ENABLE

2V002

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

3.3V

2017/6/5
AL: 104 4787960 C08

2.49A

$$V_{out} = 0.6 \times (R2450 + R2451) / R2451 = 0.6 \times (200k + 44.2k) / 44.2k = 3.31V$$

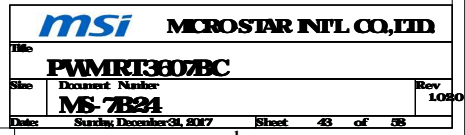
msi MICROSTAR INT'L CO., LTD.

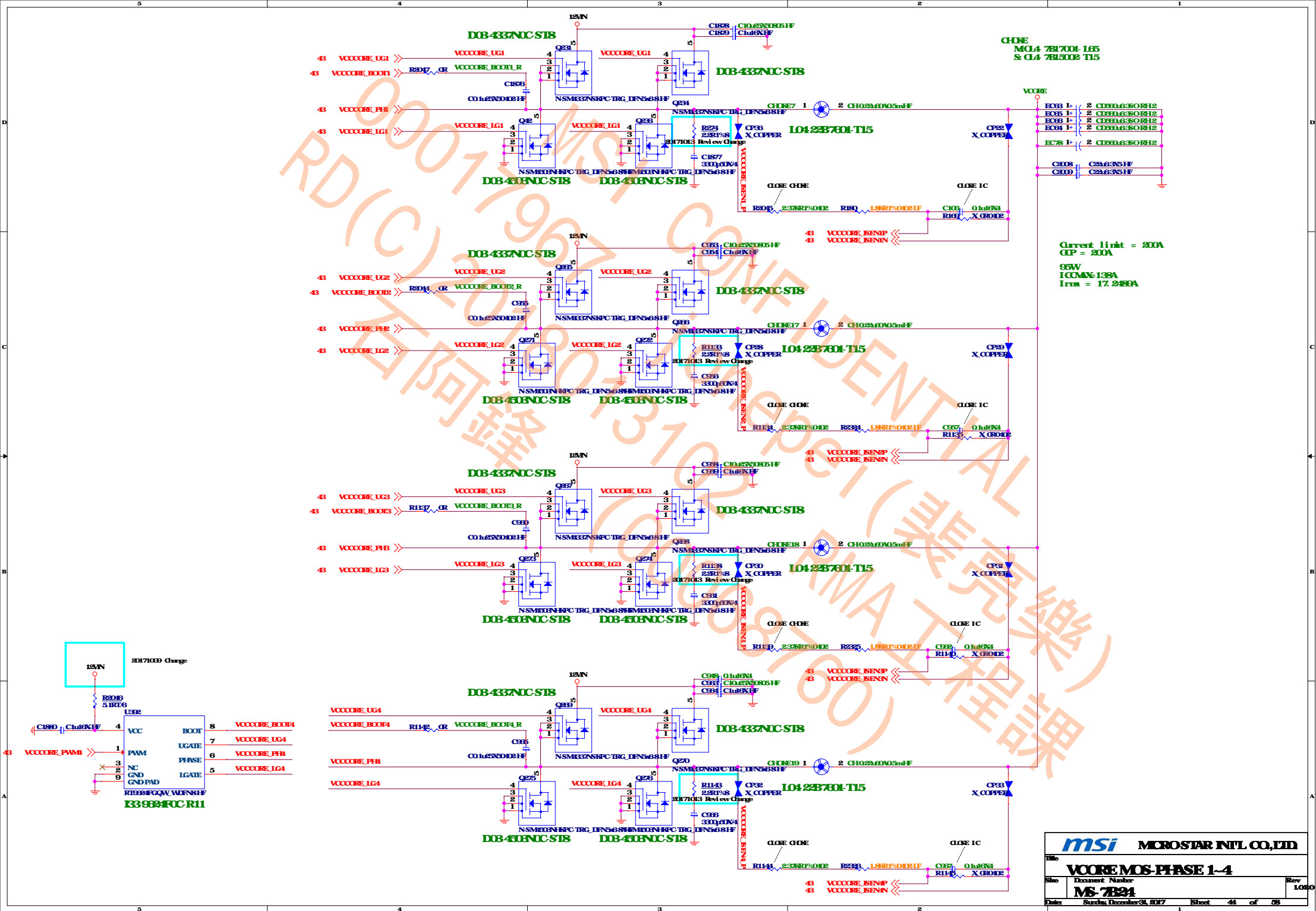
ACPI 3VSB/3MDSW

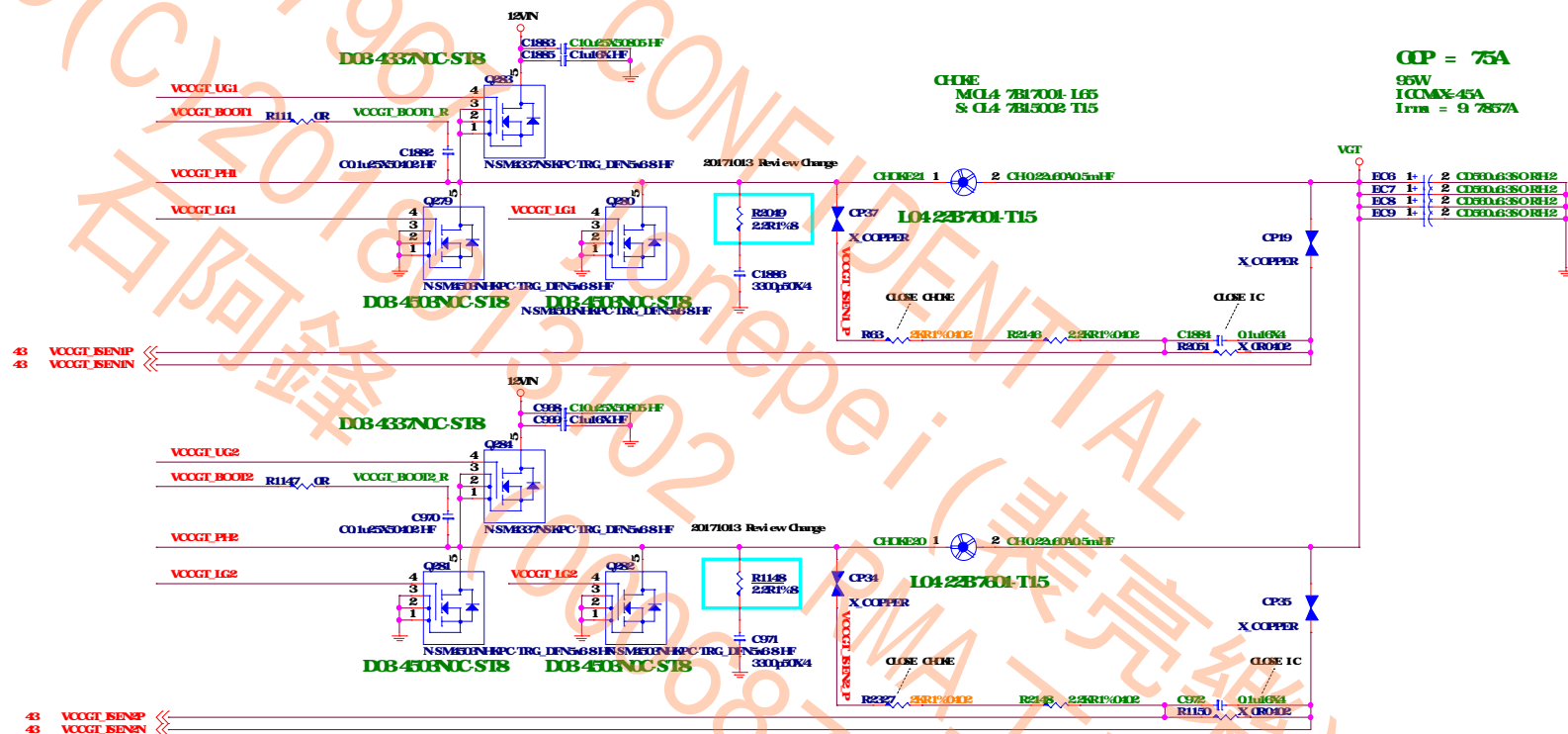
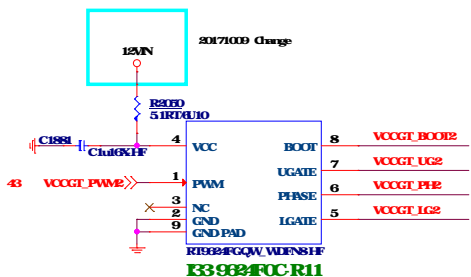
MS-7B24

Rev 1.080

Date: Sunday, December 31, 2017 Sheet: 41 of 58







SA Power: 1.05V, 123A

Rocpset: 5.6K
 OCP(min) = Rocpset * Iocset / Rison (Low side)
 = 5.1K * 10uA / 3.3mhm
 = 15.45A

OCP(max) = Rocpset * Iocset / Rison (Low side)
 = 5.1K * 10uA / 2.1mhm
 = 24.2A

OCP(test) = 19.2A

Rison (Low 10V)
 DB 632BAC N03 :
 Max 3.3mhm Type 2.1mhm

up1540 C5/R115 no stuff

2014.12.25
 for up1540 C39 is OCP set min 5K ohm
 stuff 5.3K OCP SEE 15.76A

2014.08.25 update

K38125E0CR11

$$V_{out} = V_{ref} * (R2057 + R2058) / R2058$$

$$= 0.8 * (1k + 3.16k) / 3.16k$$

$$= 1.053V$$

$$I_{rms} = I_{out} * \sqrt{R_{DS(on)} * (V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 18 * 0.2825$$

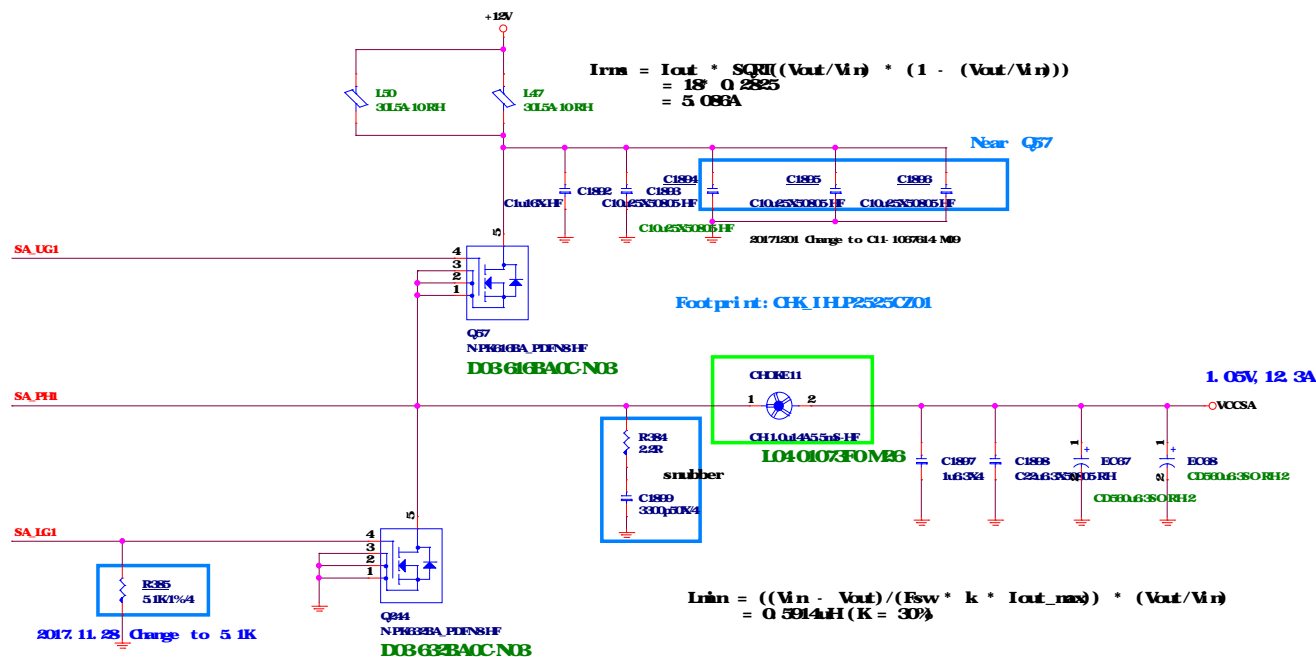
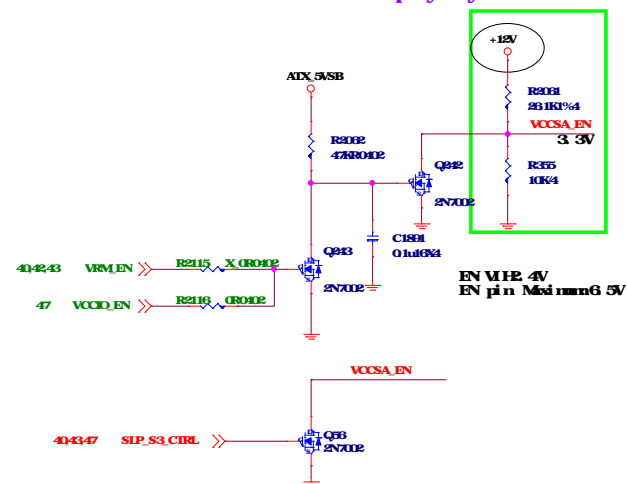
$$= 5.086A$$

Footprint: CH11HP2525C201

$$I_{lim} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.5914uH (K = 30\%)$$

R11 up by layout & Check Level

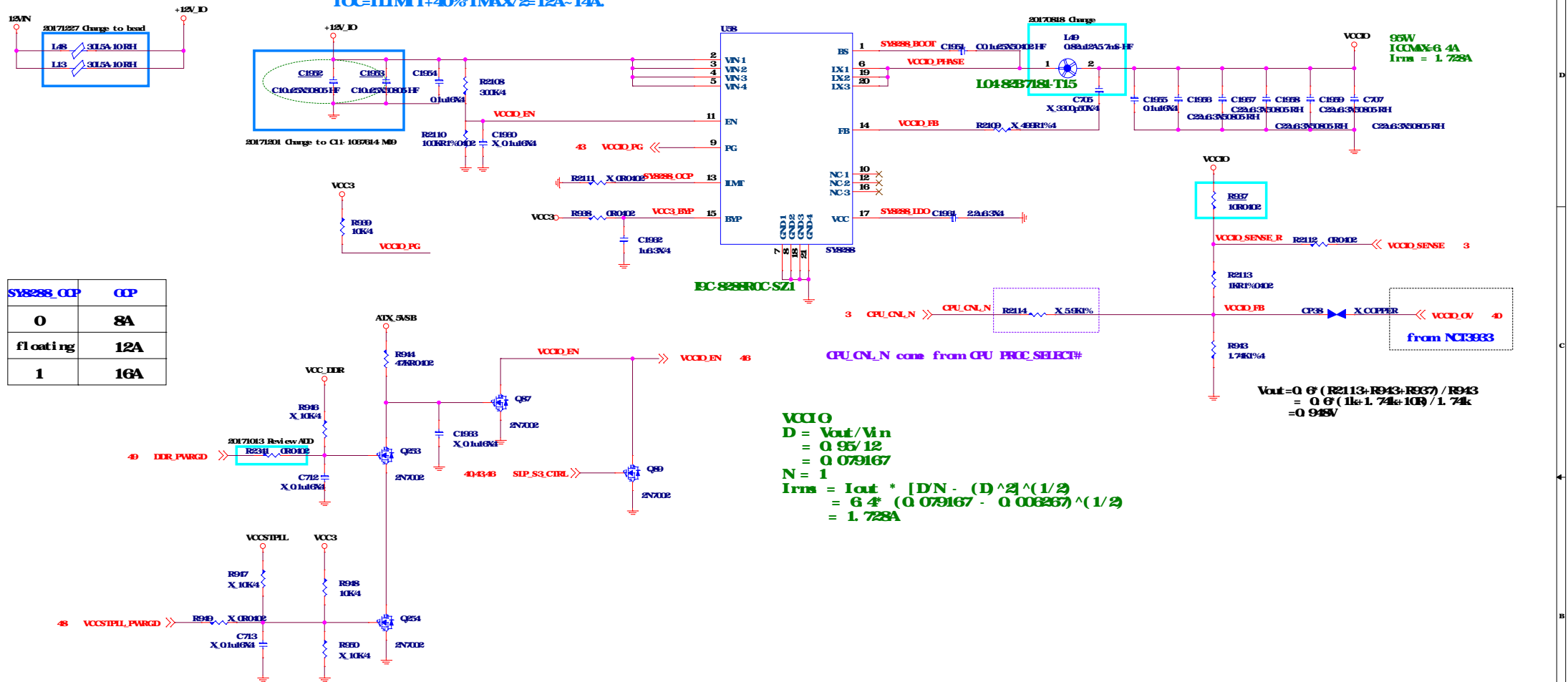


SLP_S3# assertion to VCC, VCCG, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled max 1us

IO Power: 0.95V, 64A

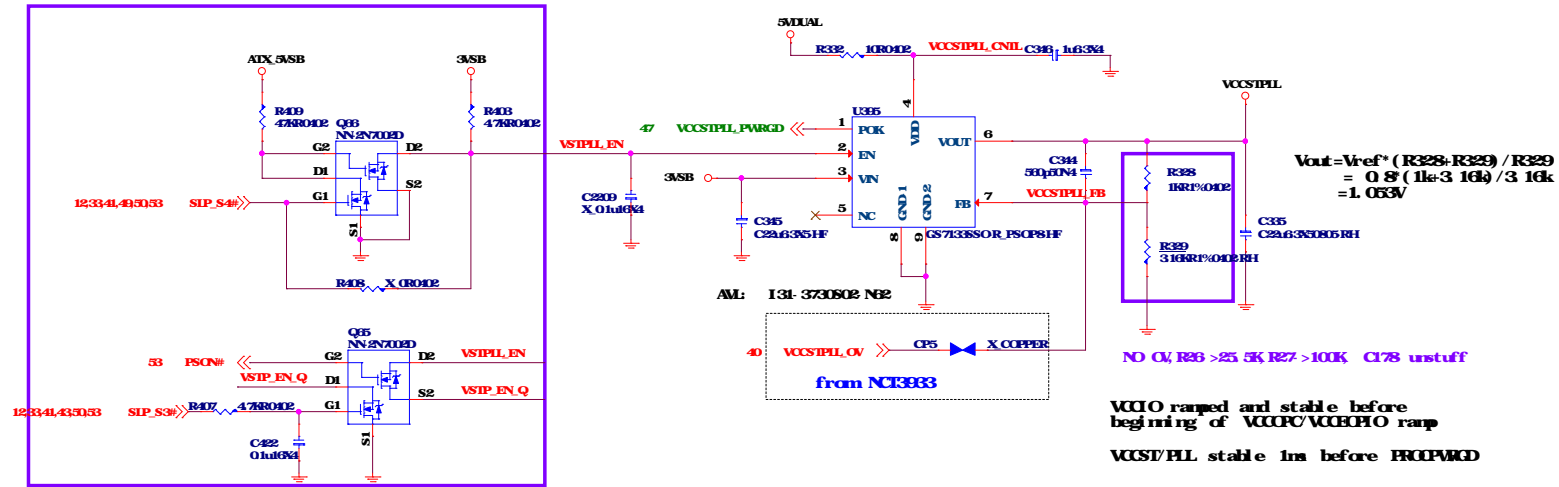
IMAX 10A
ILIMIT=10A-12A
IOC=ILIMIT+40% IMAX/2-12A-14A



VCCSTPLL

1.05V, 230mA

For Cost down VCCST&CCPLL merge

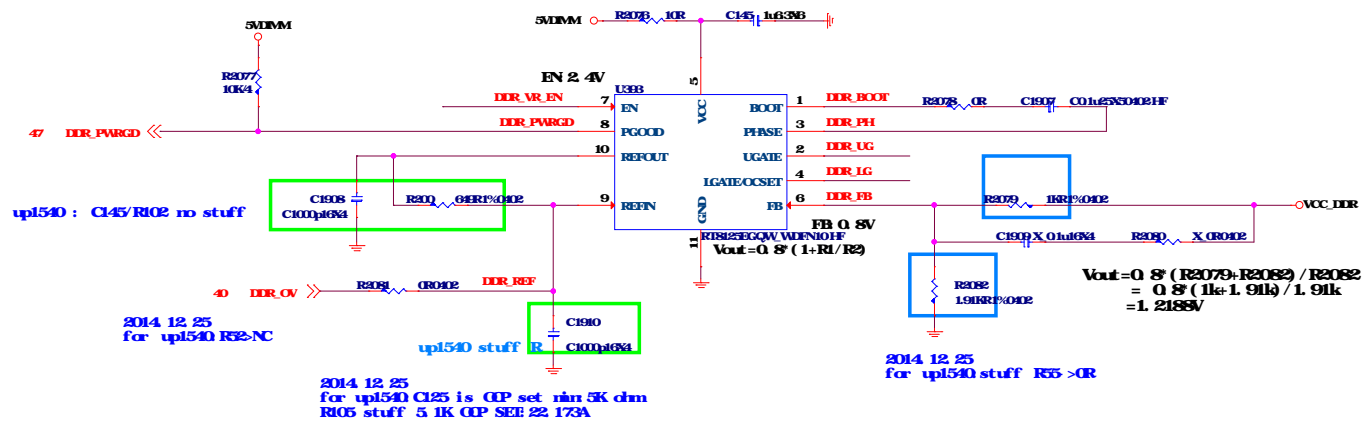


1.2A FOR DDR VTT

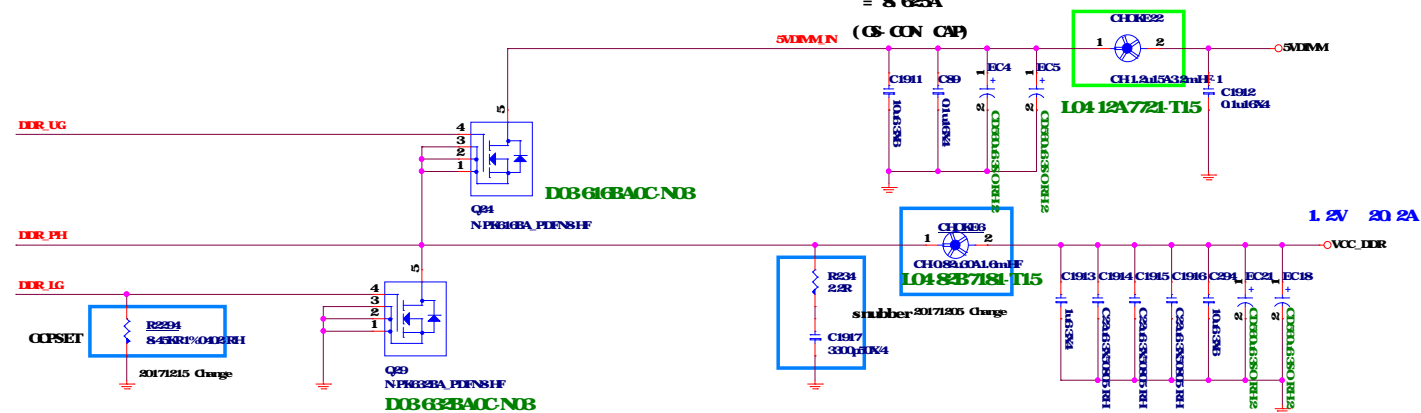
$R_{ocset} = 6 \text{ } 04K$
 $QIP_{(type)} = R_{ocset} * I_{ocset} / R_{lson}(Low \text{ side})$
 $= 8 \text{ } 45K \text{ } 10uA / 4 \text{ } 6mA$
 $= 18 \text{ } 3A$
 $QIP_{(max)} = R_{ocset} * I_{ocset} / R_{lson}(Low \text{ side})$
 $= 8 \text{ } 45K \text{ } 10uA / 3mA$
 $= 28 \text{ } 2A$

OOP(test) = 23.4A

Rdson(low) 4.5V
IDB 632BA0C N03 :
MAX 4.6nA/m TYPE 3nA/m

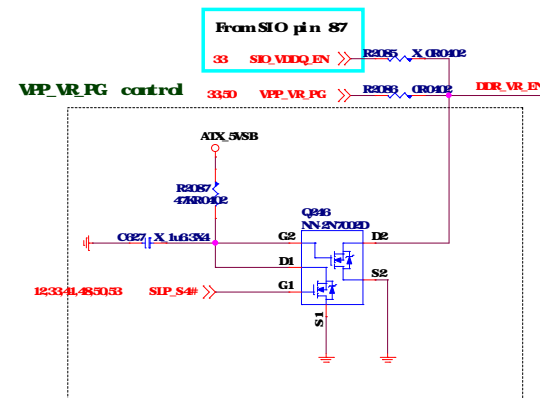


$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{0.5 * (V_{out}/V_{in}) * [1 + (V_{out}/V_{in})]} \\ &= 20.2 * 0.427 \\ &= 8.625A \end{aligned}$$



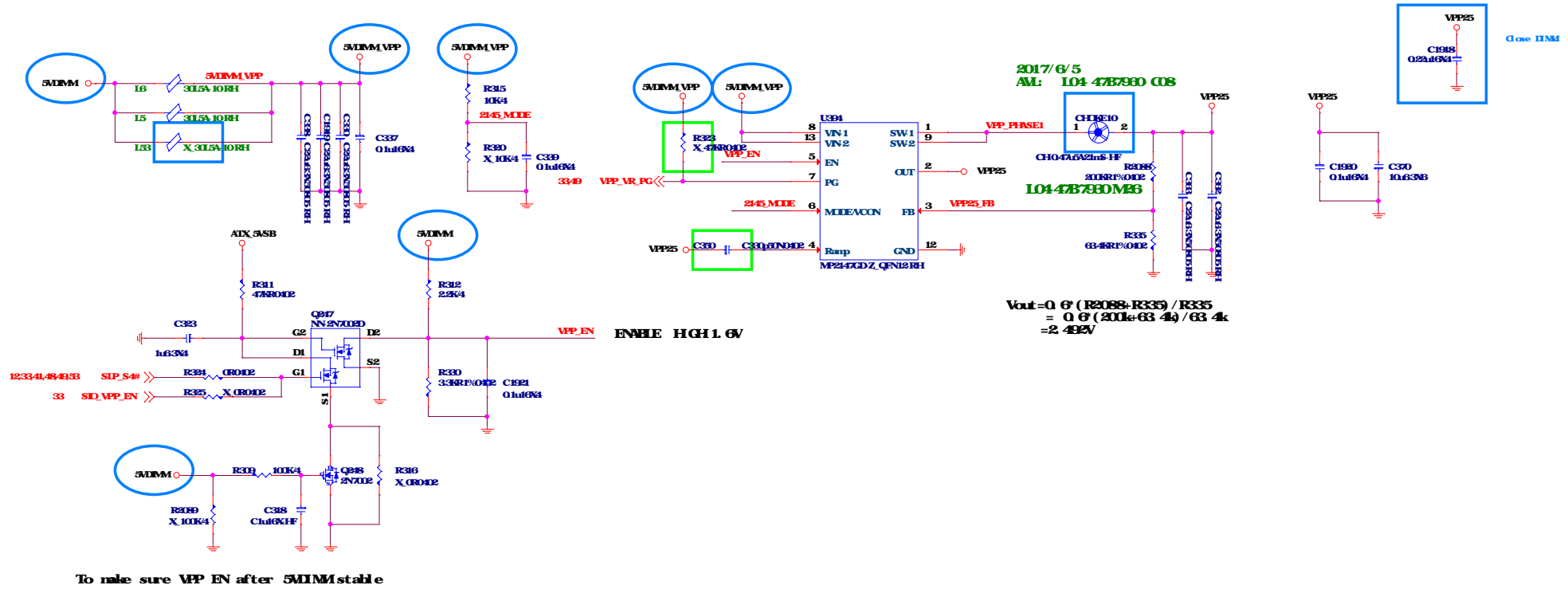
Datasheet
 $I_{min} = ((V_{in} - 1.2V) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$
 $= 0.7677A (K = 30\%)$

CAPR, 0.232H L 1.289 WH

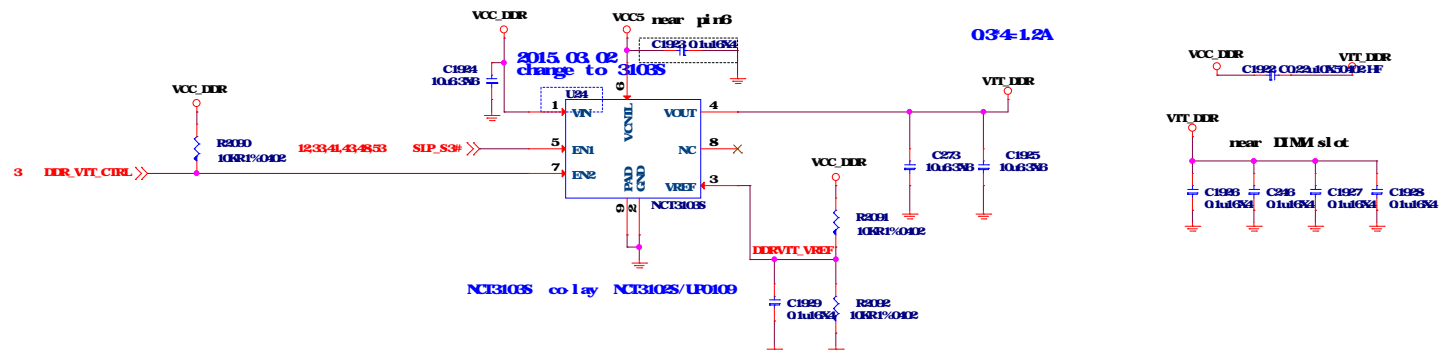


4DIMM:2 24A FOR DDR VPP2.5V

VPP25 Power
2 5V; 2 24A



DDR VTT Power



PCH 1VSB

1.05V 11.576A

Rocpset: 6.04K
 $OCF(type) = Rocpset * 10uA / Rlsor(LOW side)$
 $= 5.6K * 10uA / 4.6uA$
 $= 12.1A$
 $OCF(max) = Rocpset * 10uA / Rlsor(LOW side)$
 $= 5.6K * 10uA / 3uA$
 $= 18.6A$

OCF(test) = 17.16A

Rlsor(LOW) 4.5V
 DB 632BAC N03 :
 MAX 4.6uA TYPE 3uA

40 PCHCORE_OV
 to sink/source over voltage IC
 pin10 sink/source current capability can't over 1mA
 So max voltage can't over 1.5V
 from NCI3933

$$I_{rms} = I_{out} * \sqrt{SQRT(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.68A * 0.4$$

$$= 4.2656A < 5000mA$$

L04 47B730 T15 for OC Gating 10 9 7 5
 L04 12A7321-165 for Gating 3 SLI, ECO
 L04 12A721-115 for cost down

L1=13 11A 1.05V/0.8/5V=3.44A
 L02 3008043 M26

MAX 11.576A

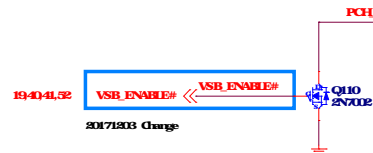
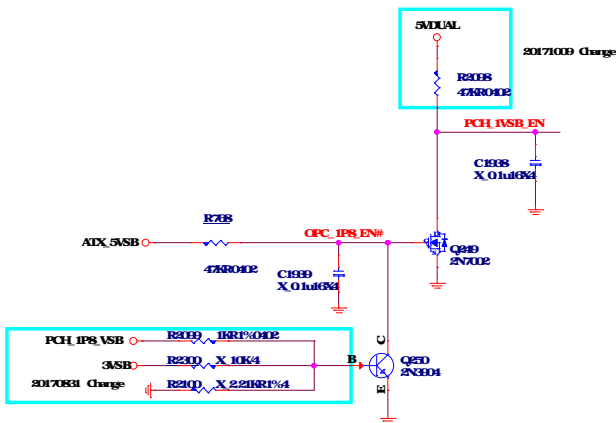
$$I_{lim} = ((V_{in} - V_{out}) / (f_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

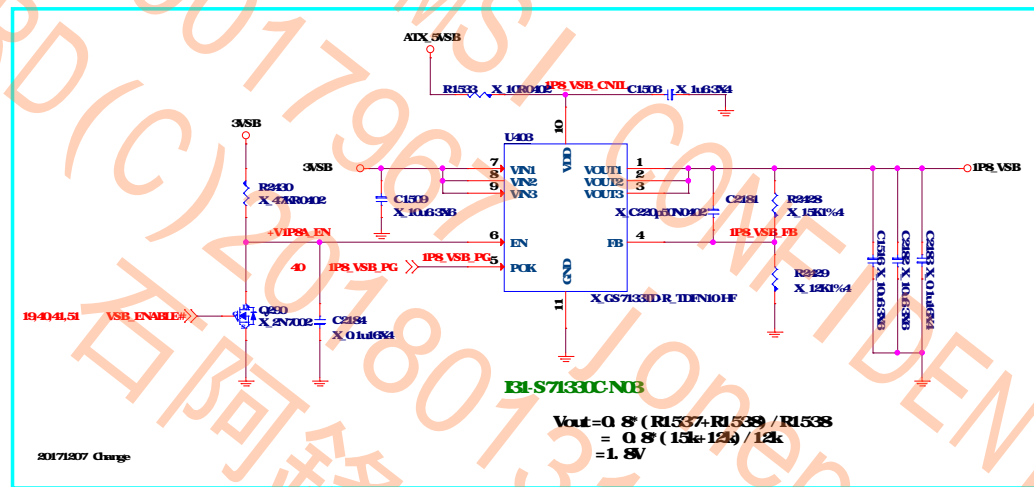
$$= 0.8335uH (K = 30\%)$$

$$V_{out} = V_{ref} * (((R2097 - R750) / R750))$$

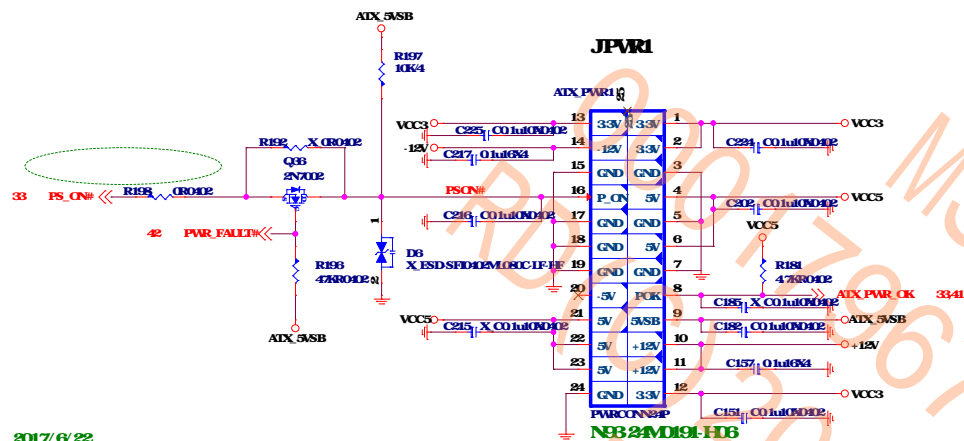
$$= 0.8 * (((3.16K - 1K) / 3.16K))$$

$$= 1.053V$$



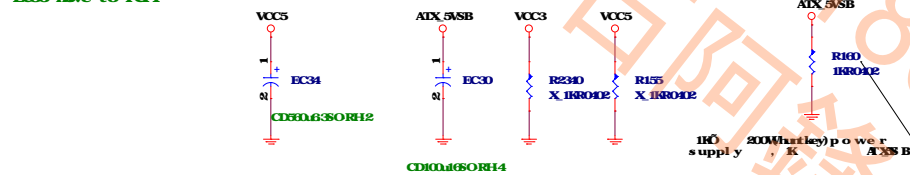


ATX POWER CONNECTOR

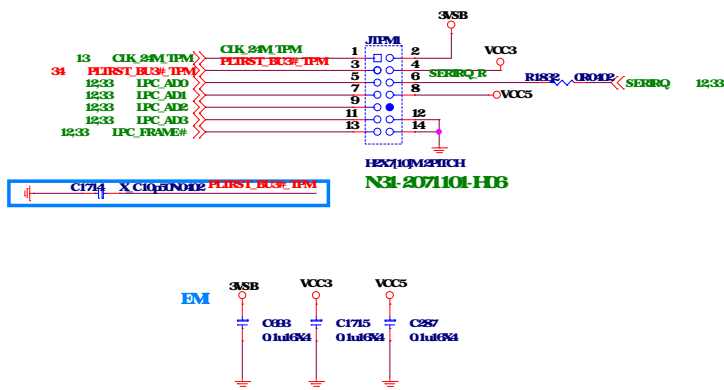


2017/6/22
EC34, EC36 are changed from 470uF to 560uF by buyer request

2017/ 7/ 6
EC36 move to PCI 1

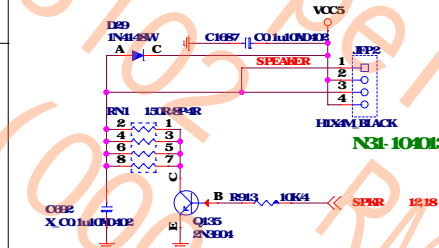
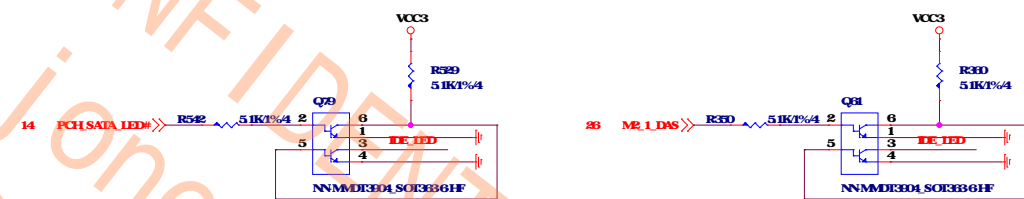
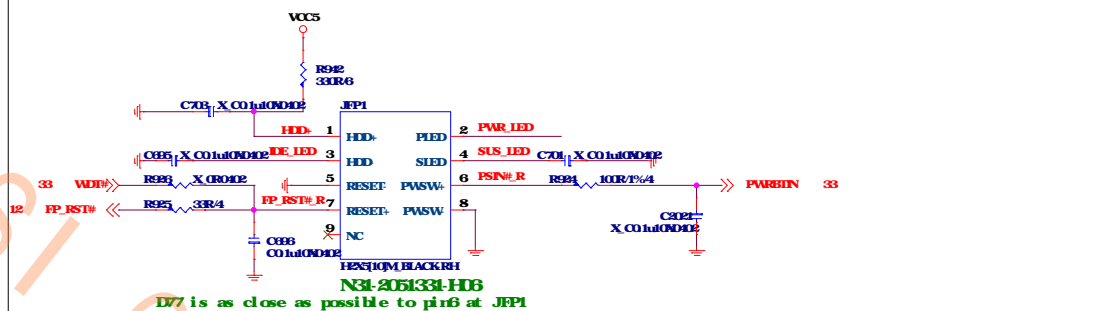


TPMPi n Header

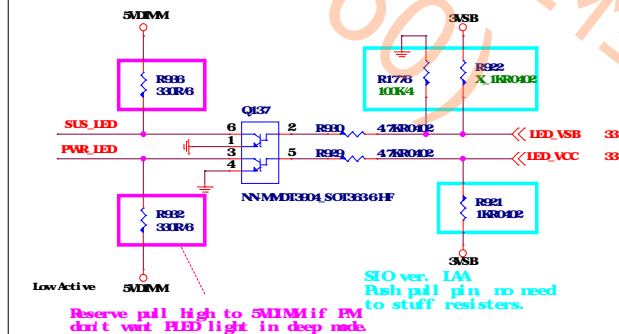


3

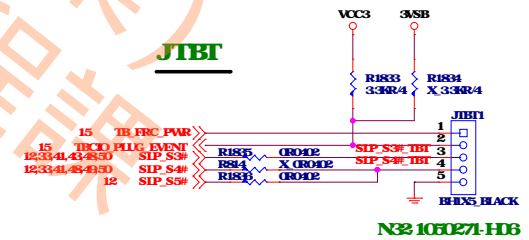
FRONT PANNEL



Front Panel LED



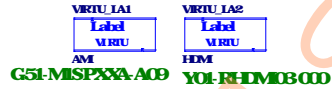
ЖТБГ





E21-788000 F02

D060100101-P01



G51-MISPAXA-A09 Y01-RHDM03000



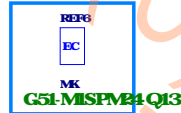
FOR PRO



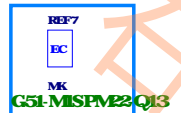
7834.0A

PDO- 07B240A- G37, (MS)
PDO- 07B240A- E48, (MS)

FOR BAZOOKA H370

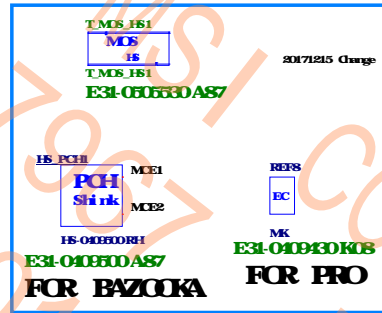


G51-MISPM24 Q13

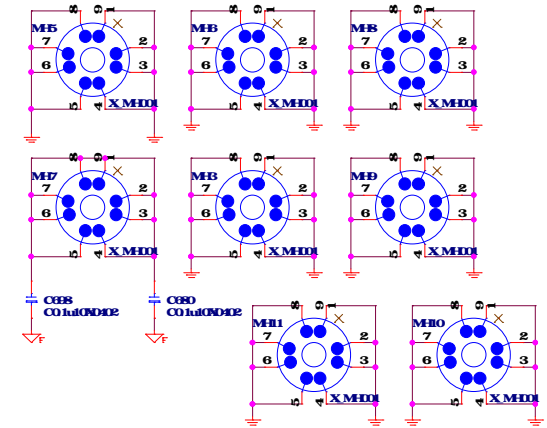


G51-MISPM22 Q13

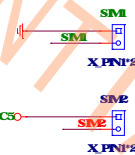
FOR BAZOOKA B360



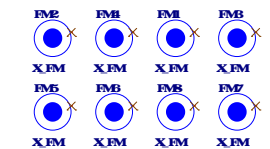
Mounting Holes



Simulation



Optical Fiducial Marks- 120



Vcheck

